List of 624 patents owned by Rambus, compiled by sabatino Dec 26 2008

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Method and apparatus for fail-safe resynchronization with minimum latency
448 6,470,405

Protocol for communication with dynamic memory
449 6,469,555

Apparatus and method for generating multiple clock signals from a single loop circuit
450 6,462,591

Semiconductor memory device having a controlled output driver characteristic
451 6,462,588

Asymmetry control for an output driver
452 6,453,401

Memory controller with timing constraint tracking and checking unit and corresponding method
453 6,452,863

Method of operating a memory device having a variable data input length
454 6,449,159

Semiconductor module with imbedded heat spreader
455 6,448,828

Apparatus and method for edge based duty cycle conversion
456 6,448,813

Output driver circuit with well-controlled output impedance
457 6,447,321

Socket for coupling an integrated circuit package to a printed circuit board
458 6,426,984

Apparatus and method for reducing clock signal phase skew in a master-slave system with multiple latent clock cycles
459 6,426,916

Memory device having a variable data output length and a programmable register
460 6,415,339

Memory device having a plurality of programmable internal registers and a delay time register
461 6,405,296
Asynchronous request/synchronous data dynamic random access memory

462 6,404,660
Semiconductor package with a controlled impedance bus and method of forming same

463 6,401,167
High performance cost optimized memory

464 6,396,887
Apparatus and method for generating a distributed clock signal using gear ratio techniques

465 6,396,329
Method and apparatus for receiving high speed signals with low latency

466 6,384,637
Differential amplifier with selectable hysteresis and buffered filter

467 6,378,020
System having double data transfer rate and integrated circuit therefor

468 6,378,018
Memory device and system including a low power interface

469 6,376,904
Redistributed bond pads in stacked integrated circuit die package

470 6,373,768
Apparatus and method for thermal regulation in memory subsystems

471 6,373,293
Self-synchronized, multi-sample, quadrature phase detector

472 6,370,668
High speed memory system capable of selectively operating in non-chip-kill and chip-kill modes

473 6,369,652
Differential amplifiers with current and resistance compensation elements for balanced output

474 6,369,626
Low pass filter for a delay locked loop circuit

475 6,359,931
Apparatus and method for multilevel signaling
476 6,356,975

Apparatus and method for pipelined memory operations
477 6,352,435

Chip socket assembly and chip file assembly for semiconductor chips
478 6,349,050

Methods and systems for reducing heat flux in memory systems
479 6,347,354

Apparatus and method for maximizing information transfers over limited interconnect resources
480 6,345,009

Apparatus and method for refreshing subsets of memory devices in a memory system
481 6,343,352

Method and apparatus for two step memory write operations
482 6,343,042

DRAM core refresh with reduced spike current
483 6,342,800

Charge compensation control circuit and method for use with output driver
484 6,340,909

Method and apparatus for phase interpolation
485 6,340,900

Phase detector with minimized phase detection error
486 6,330,193

Method and apparatus for low capacitance, high output impedance driver
487 6,324,120

Memory device having a variable data output length
488 6,323,706

Apparatus and method for edge based duty cycle conversion
489 RE37,452

At frequency phase shifting circuit for use in a quadrature clock generator
Apparatus and method for topography dependent signaling

Memory device having write latency

Rambus DRAM (RDRAM) apparatus and method for performing refresh operations

Electronically moveable terminator and method for using same in a memory system

Memory and method for sensing sub-groups of memory elements

Method of operation of a memory controller

Method and apparatus for reducing worst case power

Current control technique

Connector with staggered contact design

Memory controller and method for memory devices with multiple banks of memory cells

Multi-slot connector with integrated bus providing contact between adjacent modules

Method and apparatus for providing a memory with write enable information

High-frequency bus system

DRAM core refresh with reduced spike current
Method of operating a memory device having write latency
505 6,263,448

Power control system for synchronous memory device
506 6,260,097

Method and apparatus for controlling a synchronous memory device
507 6,234,820

Method and apparatus for joining printed circuit boards
508 6,232,796

Apparatus and method for detecting two data bits per clock edge
509 6,226,757

Apparatus and method for bus timing compensation
510 6,226,754

Apparatus and method for device timing compensation
511 6,209,071

Asynchronous request/synchronous data dynamic random access memory
512 6,205,191

Method and apparatus for synchronizing a control signal
513 6,204,697

Low-latency small-swing clocked receiver
514 6,198,307

Output driver circuit with well-controlled output impedance
515 6,185,644

Memory system including a plurality of memory devices and a transceiver device
516 6,182,184

Method of operating a memory device having a variable data input length
517 6,178,130

Apparatus and method for refreshing subsets of memory devices in a memory system
518 6,169,434

Conversion circuit with duty cycle correction for small swing signals, and associated method
Impedance controlled output driver

Motherboard having one-between trace connections for connectors

Method and apparatus for initializing dynamic random access memory (DRAM) devices by levelizing a read domain

Data packet with embedded mask

Apparatus for sharing sense amplifiers between memory banks

Variable delay element

Synchronous memory device utilizing request protocol and method of operation of same

Dependent bank memory controller method and apparatus

Delay-locked loop circuitry for clock delay adjustment

Protocol for communication with dynamic memory

Circuit and method for column redundancy for high bandwidth memories

Data packet with embedded mask

Phase interpolator with noise immunity

Zero power reset circuit for low voltage CMOS circuits
Method of operating a synchronous memory device
534 6,094,075
Current control technique
535 RE36,781
Differential comparator for amplifying small swing signals to a full swing output
536 6,085,284
Method of operating a memory device having a variable data output length and an identification register
537 6,075,744
Dram core refresh with reduced spike current
538 6,075,743
Method and apparatus for sharing sense amplifiers between memory banks
539 6,075,730
High performance cost optimized memory with delayed memory writes
540 6,070,222
Synchronous memory device having identification register
541 6,067,594
High frequency bus system
542 6,067,592
System having a synchronous memory device
543 6,049,846
Integrated circuit having memory which synchronously samples information with respect to external clock signals
544 6,047,346
System for adjusting slew rate on an output of a drive circuit by enabling a plurality of pre-drivers and a plurality of output drivers
545 6,044,426
Memory system having memory devices each including a programmable internal register
546 6,038,195
Synchronous memory device having a delay time register and method of operating same
547 6,035,369
Method and apparatus for providing a memory with write enable information
Dual clocked synchronous memory device having a delay time register and method of operating same

Method of operating a memory having a variable data output length and a programmable register

Synchronous memory device utilizing two external clocks

Method of operating a synchronous memory device having a variable data output length

Apparatus and method for thermal regulation in memory subsystems

Phase detector using switched capacitors

Method and apparatus for setting a current of an output driver for the high speed bus

Chip socket assembly and chip file assembly for semiconductor chips

Apparatus and method for multilevel signaling

Integrated circuit package for coupling to a printed circuit board

Synchronous memory device

Method and apparatus for N choose M device selection

Method and apparatus for externally configuring and modifying the transaction request response characteristics of a semiconductor device coupled to a bus

Low-latency small-swing clocked receiver
Protocol for communication with dynamic memory

Bus driver circuit including a slew rate indicator circuit having a one shot circuit

Method and apparatus for writing to memory components

Synchronous memory device having an internal register

Synchronous memory device having a programmable register and method of controlling same

Circuitry for the delay adjustment of a clock signal

Method and apparatus for writing to memory components

Memory module having memory devices containing internal device ID registers and method of initializing same

Integrated circuit I/O using a high performance bus interface

Protocol for communication with dynamic memory

Connector with integral transmission line bus

Transmitting memory requests for multiple block format memory operations the requests comprising count information, a mask, and a second mask

Method and apparatus for transmitting memory requests by transmitting portions of count data in adjacent words of a packet

Differential charge pump circuit with high differential and low common mode impedance
Current mode interface circuitry for an IC test device  
577 5,844,855

Method and apparatus for writing to memory components  
578 5,841,715

Integrated circuit I/O using high performance bus interface  
579 5,841,580

Integrated circuit I/O using a high performance bus interface  
580 5,825,209

Quadrature phase detector  
581 5,809,263

Integrated circuit I/O using a high performance bus interface  
582 5,808,498

At frequency phase shifting circuit for use in a quadrature clock generator  
583 5,799,051

Delay stage circuitry for a ring oscillator  
584 5,765,020

Method of transferring data by transmitting lower order and upper order memory address bits in separate words with respective op codes and start information  
585 5,764,963

Method and apparatus for performing maskable multiple color block writes  
586 5,748,914

Protocol for communication with dynamic memory  
587 5,748,554

Memory and method for sensing sub-groups of memory elements  
588 5,736,892

Differential charge pump circuit with high differential impedance and low common mode impedance  
589 5,715,407

Process and apparatus for collision detection on a parallel bus by monitoring a first line of the bus during even bus cycles for indications of overlapping packets  
590 5,680,361
Method and apparatus for writing to memory components
591 5,663,661

Modular bus with single or double parallel termination
592 5,657,481

Memory device with a phase locked loop circuitry
593 5,638,334

Integrated circuit I/O using a high performance bus interface
594 5,621,340

Differential comparator for amplifying small swing signals to a full swing output
595 5,614,855

Delay-locked loop
596 5,606,717

Memory circuitry having bus interface for receiving information in packets and access time registers
597 5,596,610

Delay stage circuitry for a ring oscillator
598 5,578,940

Modular bus with single or double parallel termination
599 5,572,158

Amplifier with active duty cycle correction
600 5,554,945

Voltage controlled phase shifter with unlimited range
601 5,537,573

Cache system and method for prefetching of data
602 5,513,327

Integrated circuit I/O using a high performance bus interface
603 5,511,024

Dynamic random access memory system
604 5,499,385

Method for accessing and transmitting data to/from a memory in packets
605 5,499,355
Prefetching into a cache to minimize main memory access time and cache size in a computer system

606 5,488,321
Static high speed comparator

607 5,485,490
Method and circuitry for clock synchronization

608 5,473,575
Integrated circuit I/O using a high performance bus interface

609 5,451,898
Bias circuit and differential amplifier having stabilized output swing

610 5,446,696
Method and apparatus for implementing refresh in a synchronous DRAM system

611 5,434,817
Dynamic random access memory system

612 5,432,823
Method and circuitry for minimizing clock-data skew in a bus system

613 5,430,676
Dynamic random access memory system

614 5,422,529
Differential charge pump circuit with high differential and low common mode impedance

615 5,408,129
Integrated circuit I/O using a high performance bus interface

616 5,390,308
Method and apparatus for address mapping of dynamic random access memory

617 5,357,195
Testing set up and hold input timing parameters of high speed integrated circuit devices

618 5,355,391
High speed bus system

619 5,337,285
Method and apparatus for power control in devices

620 5,325,053

Apparatus for testing timing parameters of high speed integrated circuit devices

621 5,319,755

Integrated circuit I/O using high performance bus interface

622 5,268,639

Testing timing parameters of high speed integrated circuit devices

623 5,254,883

Electrical current source circuitry for a bus

624 5,243,703

Apparatus for synchronously generating clock signals in a data processing system