List of 624 patents owned by Rambus, compiled by sabatino Dec 26 2008

1 7,467,320

Fault-tolerant clock generator

2 7,466,784

Apparatus and method for controlling a master/slave system via master device synchronization

3 7,464,225

Memory module including a plurality of integrated circuit memory devices and a plurality of buffer devices in a matrix topology

4 7,461,192

Interface for bridging out-of-band information and preventing false presence detection of terminating devices

5 7,460,565

Data communications circuit with multi-stage multiplexing

6 7,457,117

System for controlling the temperature of electronic devices

7 7,456,778

Method and apparatus for calibrating a multi-level current mode driver having a plurality of source calibration signals

8 7,454,555

Apparatus and method including a memory device having multiple sets of memory banks with duplicated data emulating a fast access time, fixed latency memory device

9 7,450,629

Adjustable dual-band link

10 7,450,535

Pulsed signaling multiplexer

11 7,448,397

Apparatus for applying disparate etching solutions to interior and exterior surfaces

12 7,444,577

Memory device testing to support address-differentiated refresh rates

13 7,443,941

Method and system for phase offset cancellation in systems using multi-phase clocks

14 7,439,789

Systems and methods for controlling termination resistance values for a plurality of communication channels

15 7,439,760

Configurable on-die termination

16 7,437,527

Memory device with delayed issuance of internal write command

17 7,433,397

Partial response receiver with clock data recovery

18 7,423,454

High speed signaling system with adaptive transmit pre-emphasis

19 7,421,548

Memory system and method for two step memory write operations

20 7,420,990

Adaptive-allocation of I/O bandwidth using a configurable interconnect topology

21 7,420,874

Integrated circuit memory device, system and method having interleaved row and column control

22 7,417,871

Memory module

23 7,415,073

Communication channel calibration for drift conditions

24 7,414,489

Phase controlled oscillator circuit with input signal coupler

25 7,412,016

Data-level clock recovery

26 7,408,995

High speed communication system with a feedback synchronization loop

27 7,408,981

Methods and circuits for performing margining tests in the presence of a decision feedback equalizer

28 7,408,378

Calibration methods and circuits for optimized on-die termination

29 7,404,032

Configurable width buffered module having switch elements

30 7,400,671

Periodic calibration for communication channels by drift tracking

31 7,400,670

Periodic calibration for communication channels by drift tracking

32 7,398,413

Memory device signaling system and method with independent timing calibration for parallel signal paths

33 7,398,333

Integrated circuit input/output interface with empirically determined delay matching

34 7,397,848

Partial response receiver

35 7,397,725

Single-clock, strobeless signaling system

36 7,392,492

Multi-format consistency checking tool

37 7,389,194

Driver calibration methods and circuits

38 7,380,092

Memory device and system having a variable depth write buffer and preload method

39 7,370,152

Memory controller with prefetching capability

40 7,369,444

Early read after write operation memory device, system and method

41 7,368,961

Clock distribution network supporting low-power mode

42 7,366,275

Output calibrator with dynamic precision

43 7,365,581

Regulated adaptive-bandwidth PLL/DLL using self-biasing current from a VCO/VCDL

44 7,363,422

Configurable width buffered module

45 7,362,800

Auto-configured equalizer

46 7,362,626

Asynchronous, high-bandwidth memory component using calibrated timing elements

47 7,362,130

Method and device for transmission with reduced crosstalk

48 7,360,187

Mixed mode verifier

49 7,360,127

Method and apparatus for evaluating and optimizing a signaling system

50 7,360,050

Integrated circuit memory device having delayed write capability

51 7,356,639

Configurable width buffered module having a bypass circuit

52 7,353,357

Apparatus and method for pipelined memory operations

53 7,352,234

Current control technique

54 7,349,510

Apparatus for data recovery in a synchronous chip-to-chip system

55 7,349,484

Adjustable dual-band link

56 7,349,279

Memory Device Having a Configurable Oscillator for Refresh Operation

57 7,348,811

Equalizing transceiver with reduced parasitic capacitance

58 7,346,819

Through-core self-test with multiple loopbacks

59 7,337,294

Method and apparatus for adjusting the performance of a synchronous memory system

60 7,336,749

Statistical margin test methods and circuits

61 7,331,006

Multiple sweep point testing of circuit devices

62 7,330,953

Memory system having delayed write timing

63 7,330,952

Integrated circuit memory device having delayed write timing based on read response time

64 7,330,951

Apparatus and method for pipelined memory operations

65 7,321,524

Memory controller with staggered request signal output

66 7,320,082

Power control system for synchronous memory device

67 7,320,047

System having a controller device, a buffer device and a plurality of memory devices

68 7,319,345

Wide-range multi-phase clock generator

69 7,315,929

Memory device

70 7,313,639

Memory system and device with serialized data transfer

71 7,308,065

Delay locked loop circuitry for clock delay adjustment

72 7,308,058

Transparent multi-mode PAM interface

73 7,308,048

System and method for selecting optimal data transition types for clock and data recovery

74 7,308,044

Technique for receiving differential multi-PAM signals

75 7,307,560

Phase linearity test circuit

76 7,307,461

System and method for adaptive duty cycle optimization

77 7,302,631

Low overhead coding techniques

78 7,301,831

Memory systems with variable delays for write data signals

79 7,298,807

Circuit, apparatus and method for adjusting a duty-cycle of a clock signal in response to incoming serial data

80 7,292,637

Noise-tolerant signaling schemes supporting simplified timing and data recovery

81 7,292,629

Selectable-tap equalizer

82 7,288,973

Method and apparatus for fail-safe resynchronization with minimum latency

83 7,287,119

Integrated circuit memory device with delayed write command processing

84 7,287,109

Method of controlling a memory device having a memory core

85 7,285,443

Stacked semiconductor module

86 RE39,879

Method of transferring data by transmitting lower order and upper order memory address bits in separate words with

respective op codes and start information

87 7,280,428

Multi-column addressing mode memory system including an integrated circuit memory device

88 7,275,171

Method and apparatus for programmable sampling clock edge selection

89 7,274,244

Pulse multiplexed output system

90 7,274,242

Pass transistors with minimized capacitive loading

91 7,271,623

Low-power receiver equalization in a clocked sense amplifier

92 7,269,708

Memory controller for non-homogenous memory system

93 7,269,212

Low-latency equalization in multi-level, multi-line communication systems

94 7,268,706

Low power, DC-balanced serial link transmitter

95 7,268,605

Technique for operating a delay circuit

96 7,268,602

Method and apparatus for accommodating delay variations among multiple signals

97 7,266,634

Configurable width buffered module having flyby elements

98 7,263,149

Apparatus and method for generating a distributed clock signal

99 7,257,183

Digital clock recovery circuit

100 7,254,797

Input/output cells with localized clock routing

101 7,254,075

Integrated circuit memory system having dynamic memory bank count and page size

102 7,248,086

Leakage compensation for capacitors in loop filters

103 7,246,274

Method and apparatus for estimating random jitter (RJ) and deterministic jitter (DJ) from bit error rate (BER)

104 7,236,894

Circuits, systems and methods for dynamic reference voltage calibration

105 7,233,164

Offset cancellation in a multi-level signaling system

106 7,231,306

Method and apparatus for calibrating static timing offsets across multiple outputs

107 7,225,311

Method and apparatus for coordinating memory operations among diversely-located memory components

108 7,225,292

Memory module with termination component

109 7,222,224

System and method for improving performance in computer memory systems supporting multiple memory access latencies

110 7,222,209

Expandable slave device system

111 7,219,205

Memory controller device

112 7,216,187

Memory system including a circuit to convert between parallel and serial bits

113 7,215,161

Wave shaping output driver to adjust slew rate and/or pre-emphasis of an output signal

114 7,213,121

Memory device having asynchronous/synchronous operating modes

115 7,210,016

Method, system and memory controller utilizing adjustable write data delay settings

116 7,210,015

Memory device having at least a first and a second operating mode

117 7,209,997

Controller device and method for operating same

118 7,209,397

Memory device with clock multiplier circuit

119 7,206,897

Memory module having an integrated circuit buffer device

120 7,206,896

Integrated circuit buffer device

121 7,200,710

Buffer device and method of operation in a buffer device

122 7,200,055

Memory module with termination component

123 7,199,728

Communication system with low power, DC-balanced serial link

124 7,199,615

High speed signaling system with adaptive transmit pre-emphasis and reflection cancellation

125 7,199,605

Method and apparatus for low capacitance, high output impedance driver

126 7,198,197

Method and apparatus for data acquisition

127 7,197,684

Single-ended transmission for direct access test mode within a differential input and output circuit

128 7,197,611

Integrated circuit memory device having write latency function

129 7,196,567

Systems and methods for controlling termination resistance values for a plurality of communication channels

130 7,196,539

Adaptive signal termination

131 7,194,155

Adaptive control for mitigating interference in a multimode transmission medium

132 7,194,056

Determining phase relationships using digital phase values

133 7,193,467

Differential amplifiers and methods of using same

134 7,190,754

Transceiver with selectable data rate

135 7,187,721

Transition-time control in a high-speed data transmitter

136 7,187,572

Early read after write operation memory device, system and method

137 7,184,483

Technique for emulating differential signaling

138 7,183,805

Method and apparatus for multi-mode driver

139 7,180,959

Technique for utilizing spare bandwidth resulting from the use of a code in a multi-level signaling system

140 7,180,958

Technique for utilizing spare bandwidth resulting from the use of a transition-limiting code in a multi-level signaling system

141 7,180,957

Technique for utilizing spare bandwidth resulting from the use of a transition-limiting code in a multi-level signaling system

142 7,177,998

Method, system and memory controller utilizing adjustable read data delay settings

143 7,176,721

Signal receiver with data precessing function

144 7,174,400

Integrated circuit device that stores a value representative of an equalization co-efficient setting

145 7,171,528

Method and apparatus for generating a write mask key

146 7,171,321

Individual data line strobe-offset control in memory systems

147 7,170,314

Multiple channel modules and bus systems using same

148 7,167,039

Memory device having an adjustable voltage swing setting

149 7,167,019

Method and device for transmission with reduced crosstalk

150 7,164,997

Bus line current calibration

151 7,164,292

Reducing electrical noise during bus turnaround in signal transfer systems

152 7,162,672

Multilevel signal interface testing with binary test apparatus by emulation of multilevel signals

153 7,162,376

Circuits, systems and methods for dynamic reference voltage calibration

154 7,161,513

Apparatus and method for improving resolution of a current mode driver

155 7,161,400

Phase synchronization for wide area integrated circuits

156 7,159,136

Drift tracking feedback for communication channels

157 7,158,536

Adaptive-allocation of I/O bandwidth using a configurable interconnect topology

158 7,154,302

Method and apparatus for selectably providing single-ended and differential signaling with controllable impedance and transition time

159 7,151,390

Calibration methods and circuits for optimized on-die termination

160 7,149,856

Method and apparatus for adjusting the performance of a synchronous memory system

161 7,148,699

Technique for calibrating electronic devices

162 7,142,612

Method and apparatus for multi-level signaling

163 7,142,475

Memory device having a configurable oscillator for refresh operation

164 7,138,877

PLL and method for providing a single/multiple adjustable frequency range

165 7,137,048

Method and apparatus for evaluating and optimizing a signaling system

166 7,136,949

Method and apparatus for position dependent data scheduling

167 7,136,310

Programmable output driver turn-on time for an integrated circuit memory device

168 7,135,925

Adaptive bias scheme for high-voltage compliance in serial links

169 7,135,903

Phase jumping locked loop circuit

170 7,134,101

Active impedance compensation

171 7,133,945

Scalable I/O signaling topology using source-calibrated reference voltages

172 7,133,463

Linear transformation circuits

173 7,130,944

Chip-to-chip communication system using an ac-coupled bus and devices employed in same

174 7,129,739

Method and apparatus for selectably providing single-ended and differential signaling with controllable impedence and transition time

175 7,127,017

Clock recovery circuit with second order digital filter

176 7,127,003

Method and apparatus for communicating information using different signaling types

177 7,126,510

Circuit calibration system and method

178 7,126,435

Voltage controlled oscillator amplitude control circuit

179 7,126,408

Method and apparatus for receiving high-speed signals with low latency

180 7,126,378

High speed signaling system with adaptive transmit pre-emphasis

181 7,124,270

Transceiver with latency alignment circuitry

182 7,124,221

Low latency multi-level communication interface

183 7,122,889

Semiconductor module

184 7,119,549

Output calibrator with dynamic precision

185 7,113,550

Technique for improving the quality of digital signals in a multi-level signaling system

186 7,110,322

Memory module including an integrated circuit device

187 7,102,390

Method and apparatus for signal reception using ground termination and/or non-ground termination

188 7,099,786

Signaling accommodation

189 7,099,424

Clock data recovery with selectable phase control

190 7,099,395

Reducing coupled noise in pseudo-differential signaling systems

191 7,095,789

Communication channel calibration for drift conditions

192 7,095,265

PVT-compensated clock distribution

193 7,093,145

Method and apparatus for calibrating a multi-level current mode driver having a plurality of source calibration signals

194 7,092,472

Data-level clock recovery

195 7,092,449

High-speed communication system with a feedback synchronization loop

196 7,091,761

Impedance controlled output driver

197 7,089,442

Fault-tolerant clock generator

198 7,088,270

Low power, DC-balanced serial link

199 7,088,127

Adaptive impedance output driver circuit

200 7,085,906

Memory device

201 7,085,872

High frequency bus system

202 7,084,681

PLL lock detection circuit using edge detection and a state machine

203 7,081,782

Locked loop with dual rail regulation

204 7,078,979

Phase controlled oscillator circuit with input signal coupler

205 7,078,790

Semiconductor stacked die devices and methods of forming semiconductor stacked die devices

206 7,076,377

Circuit, apparatus and method for capturing a representation of a waveform from a clock-data recovery (CDR) unit

207 RE39,153

Connector with integral transmission line bus

208 7,073,035

Techniques for increasing bandwidth in port-per-module memory systems having mismatched memory modules

209 7,072,415

Method and apparatus for generating multi-level reference voltage in systems using equalization or crosstalk cancellation

210 7,072,355

Periodic interface calibration for high speed communication

211 7,065,622

Transceiver with latency alignment circuitry

212 7,064,602

Dynamic gain compensation and calibration

213 7,062,597

Integrated circuit buffer device

214 7,061,406

Low power, DC-balanced serial link transmitter

215 7,061,273

Method and apparatus for multi-mode driver

216 7,057,460

Differential amplifier with adaptive biasing and offset cancellation

217 7,054,771

Bus line current calibration

218 7,051,151

Integrated circuit buffer device

219 7,051,130

Integrated circuit device that stores a value representative of a drive strength setting

220 7,051,129

Memory device having programmable drive strength setting

221 7,047,375

Memory system and method for two step memory write operations

222 7,046,078

Method and apparatus for distributed voltage compensation with a voltage driver that is responsive to feedback

223 7,046,056

System with dual rail regulated locked loop

224 7,043,599

Dynamic memory supporting simultaneous refresh and data-access transactions

225 7,042,914

Calibrated data communication system and method

226 7,039,782

Memory system with channel multiplexing of multiple memory devices

227 7,039,147

Delay locked loop circuitry for clock delay adjustment

228 7,039,118

High speed communication system with a feedback synchronization loop

229 7,038,543

Collective automatic gain control

230 7,037,757

Stacked semiconductor module

231 7,032,058

Apparatus and method for topography dependent signaling

232 7,032,057

Integrated circuit with transmit phase adjustment

233 7,031,868

Method and apparatus for performing testing of interconnections

234 7,030,657

High speed signaling system with adaptive transmit pre-emphasis and reflection cancellation

235 7,027,307

Clock routing in multiple channel modules and bus systems

236 7,026,848

Pre-driver circuit

237 7,024,502

Apparatus and method for topography dependent signaling

238 7,017,002

System featuring a master device, a buffer device and a plurality of integrated circuit memory devices

239 7,015,721

Push-pull output driver

240 7,012,812

Memory module

241 7,012,330

Integrated circuit device having I/O structures with reduced input loss

242 7,010,658

Transceiver with latency alignment circuitry

243 7,010,642

System featuring a controller device and a memory module that includes an integrated circuit buffer device and a plurality of integrated circuit memory devices

244 7,006,932

Technique for determining performance characteristics of electronic devices and systems

245 7,005,939

Input/output circuit with on-chip inductor to reduce parasitic capacitance

246 7,003,639

Memory controller with power management logic

247 7,003,618

System featuring memory modules that include an integrated circuit buffer devices

248 7,002,500

Circuit, apparatus and method for improved current distribution of output drivers enabling improved calibration efficiency and accuracy

249 7,002,367

Method and apparatus for low capacitance, high output impedance driver

250 7,000,062

System and method featuring a controller device and a memory module that includes an integrated circuit buffer device and a plurality of integrated circuit memory devices

251 6,999,516

Technique for emulating differential signaling

252 6,999,332

Semiconductor package with a controlled impedance bus and method of forming same

253 6,998,892

Method and apparatus for accommodating delay variations among multiple signals

254 6,998,889

Circuit, apparatus and method for obtaining a lock state value

255 6,990,042

Single-clock, strobeless signaling system

256 6,988,044

Bus line current calibration

257 6,987,823

System and method for aligning internal transmit and receive clocks

258 6,982,922

Single-clock, strobeless signaling system

259 6,982,587

Equalizing transceiver with reduced parasitic capacitance

260 6,980,020

Calibration methods and circuits for optimized on-die termination

261 6,977,980

Timing synchronization methods and systems for transmit parallel interfaces

262 6,976,114

Method and apparatus for simultaneous bidirectional signaling in a bus topology

263 6,975,956

Multiple sweep point testing of circuit devices

264 6,975,558

Integrated circuit device

265 6,975,160

System including an integrated circuit memory device having an adjustable output voltage setting

266 6,975,159

Method of operation in a system having a memory device having an adjustable output voltage setting

267 6,968,024

Apparatus and method for operating a master-slave system with a clock signal and a separate phase signal

268 6,967,514

Method and apparatus for digital duty cycle adjustment

269 6,965,262

Method and apparatus for receiving high speed signals with low latency

270 6,963,956

Apparatus and method for pipelined memory operations

271 6,963,232

Compensator for leakage through loop filter capacitors in phase-locked loops

272 6,961,862

Drift tracking feedback for communication channels

273 6,961,831

Techniques for increasing bandwidth in port-per-module memory systems having mismatched memory modules

274 6,960,952

Configuring and selecting a duty cycle for an output driver

275 6,960,948

System with phase jumping locked loop circuit

276 6,954,837

Consolidation of allocated memory to reduce power consumption

277 6,954,095

Apparatus and method for generating clock signals

278 6,952,431

Clock multiplying delay-locked loop for data communications

279 6,952,123

System with dual rail regulated locked loop

280 6,950,956

Integrated circuit with timing adjustment mechanism and method

281 6,949,958

Phase comparator capable of tolerating a non-50% duty-cycle clocks

282 6,937,073

Frequency multiplier with phase comparator

283 6,934,201

Asynchronous, high-bandwidth memory component using calibrated timing elements

284 6,931,467

Memory integrated circuit device which samples data upon detection of a strobe signal

285 6,928,128

Clock alignment circuit having a self regulating voltage supply

286 6,924,660

Calibration methods and circuits for optimized on-die termination

287 6,922,092

Impedance controlled output driver

288 6,922,091

Locked loop circuit with clock hold function

289 6,920,540

Timing calibration apparatus and method for a memory device signaling system

290 6,920,402

Technique for determining performance characteristics of electronic devices and systems

291 6,919,749

Apparatus and method for a digital delay locked loop

292 6,917,312

Technique for improving the quality of digital signals in a multi-level signaling system

293 6,912,620

Memory device which receives write masking information

294 6,911,853

Locked loop with dual rail regulation

295 6,909,387

Circuit, apparatus and method for improved current distribution of output drivers enabling improved calibration efficiency and accuracy

296 6,902,953

Methods of forming semiconductor stacked die devices

297 6,898,085

Multiple channel modules and bus systems using same

298 6,897,713

Method and apparatus for distributed voltage compensation with a voltage driver that is responsive to feedback

299 6,897,699

Clock distribution network with process, supply-voltage, and temperature compensation

300 6,889,304

Memory device supporting a dynamically configurable core organization

301 6,889,300

Memory system and method for two step write operations

302 6,882,593

Adjustable clock driver circuit

303 6,879,195

PLL lock detection circuit using edge detection

304 6,877,054

Method and apparatus for position dependent data scheduling

305 6,876,248

Signaling accommodation

306 6,873,939

Method and apparatus for evaluating and calibrating a signaling system

307 6,870,419

Memory system including a memory device having a controlled output driver characteristic

308 6,870,246

Method and apparatus for providing an integrated circuit cover

309 6,868,474

High performance cost optimized memory

310 6,864,896

Scalable unified memory architecture

311 6,861,916

Phase controlled oscillator circuit with input signal coupler

312 6,861,884

Phase synchronization for wide area integrated circuits

313 6,856,169

Method and apparatus for signal reception using ground termination and/or non-ground termination

314 6,854,030

Integrated circuit device having a capacitive coupling element

315 6,853,557

Multi-channel memory architecture

316 6,842,864

Method and apparatus for configuring access times of memory devices

317 6,839,393

Apparatus and method for controlling a master/slave system via master device synchronization

318 6,839,266

Memory module with offset data lines and bit line swizzle configuration

319 6,836,521

Apparatus and method for generating a distributed clock signal using gear ratio techniques

320 6,836,503

Apparatus for data recovery in a synchronous chip-to-chip system

321 6,833,984

Semiconductor module with serial bus connection to multiple dies

322 6,826,663

Coded write masking

323 6,826,657

Techniques for increasing bandwidth in port-per-module memory systems having mismatched memory modules

324 6,825,841

Granularity memory column access

325 6,819,137

Technique for voltage level shifting in input circuitry

326 6,813,722

Programmable timing module for adjusting clock in bus system

327 6,812,736

Method and apparatus for selectably providing single-ended and differential signaling with controllable impedance and transition time

328 6,810,449

Protocol for communication with dynamic memory

329 6,809,600

Dual loop phase lock loops using dual voltage supply regulators

330 6,809,569

Circuit, apparatus and method having a cross-coupled load with current mirrors

331 6,807,598

Integrated circuit device having double data rate capability

332 6,806,728

Circuit and method for interfacing to a bus channel

333 6,803,823

Circuit, apparatus and method for an adaptive voltage swing limiter

334 6,801,099

Methods for bi-directional signaling

335 6,798,243

Apparatus and method for level-shifting input receiver circuit from high external voltage to low internal supply voltage

336 6,788,594

Asynchronous, high-bandwidth memory component using calibrated timing elements

337 6,788,593

Asynchronous, high-bandwidth memory component using calibrated timing elements

338 6,785,782

Techniques for increasing bandwidth in port-per-module memory systems having mismatched memory modules

339 6,782,460

Pipelined memory controller and method of controlling access to memory devices in a memory system

340 6,782,459

Method and apparatus for controlling a read valid window of a synchronous memory device

341 6,781,416

Push-pull output driver

342 6,781,405

Adaptive signal termination

343 6,778,458

Dram core refresh with reduced spike current

344 6,775,809

Technique for determining performance characteristics of electronic systems

345 6,775,328

High-speed communication system with a feedback synchronization loop

346 6,772,351

Method and apparatus for calibrating a multi-level current mode driver

347 6,772,315

Translation lookaside buffer extended to provide physical and main-memory addresses

348 6,769,050

Techniques for increasing bandwidth in port-per-module memory systems having mismatched memory modules

349 6,765,800

Multiple channel modules and bus systems using same

350 6,760,857

System having both externally and internally generated clock signals being asserted on the same clock pin in normal and test modes of operation respectively

351 6,759,881

System with phase jumping locked loop circuit

352 6,757,789

Apparatus and method for maximizing information transfers over limited interconnect resources

353 6,754,783

Memory controller with power management logic

354 6,754,120

DRAM output circuitry supporting sequential data capture to reduce core access times

355 6,751,696

Memory device having a programmable register

356 6,742,097

Consolidation of allocated memory to reduce power consumption

357 6,731,545

Method and apparatus for reducing worst case power

358 6,731,148

Apparatus and method for generating clock signals

359 6,728,819

Synchronous memory device

360 6,727,759

Collective automatic gain control

361 6,721,226

Methods and systems for reducing heat flux in memory systems

362 6,721,189

Memory module

363 6,720,643

Stacked semiconductor module

364 6,718,431

Apparatus and method for pipelined memory operations

365 RE38,482

Delay stage circuitry for a ring oscillator

366 6,715,020

Synchronous integrated circuit device

367 6,714,431

Semiconductor package with a controlled impedance bus and method of forming same

368 6,708,248

Memory system with channel multiplexing of multiple memory devices

369 6,704,891

Method for verifying and improving run-time of a memory test

370 6,701,446

Power control system for synchronous memory device

371 6,697,295

Memory device having a programmable register

372 6,696,829

Self-resetting phase locked loop

373 6,687,780

Expandable slave device system

374 6,687,319

Spread spectrum clocking of digital signals

375 6,684,285

Synchronous integrated circuit device

376 6,684,263

Apparatus and method for topography dependent signaling

377 6,683,472

Method and apparatus for selectably providing single-ended and differential signaling with controllable impedance and transition time

378 6,681,338

Method and system for reducing signal skew by switching between multiple signal routing layers

379 6,681,288

Memory device with receives write masking information

380 6,675,272

Method and apparatus for coordinating memory operations among diversely-located memory components

381 6,674,377

Circuit, apparatus and method for improved current distribution of output drivers enabling improved calibration efficiency and accuracy

382 6,674,161

Semiconductor stacked die devices

383 6,671,836

Method and apparatus for testing memory

384 6,661,268

Charge compensation control circuit and method for use with output driver

385 6,657,871

Multiple channel modules and bus systems using same

386 6,657,468

Apparatus and method for controlling edge rates of digital signals

387 6,646,953

Single-clock, strobeless signaling system

388 6,643,790

Duty cycle correction circuit with frequency-dependent bias generator

389 6,643,787

Bus system optimization

390 6,643,752

Transceiver with latency alignment circuitry

391 6,642,760

Apparatus and method for a digital delay locked loop

392 6,642,746

Phase detector with minimized phase detection error

393 6,640,292

System and method for controlling retire buffer operation in a memory system

394 6,636,935

Techniques for increasing bandwidth in port-per-module memory systems having mismatched memory modules

395 6,636,098

Differential integrator and related circuitry

396 6,621,373

Apparatus and method for utilizing a lossy dielectric substrate in a high speed digital system

397 6,621,155

Integrated circuit device having stacked dies and impedance balanced transmission lines

398 6,619,973

Chip socket assembly and chip file assembly for semiconductor chips

399 6,618,786

Current-mode bus line driver having increased output impedance

400 6,617,871

Methods and apparatus for bi-directional signaling

401 6,608,507

Memory system including a memory device having a controlled output driver characteristic

402 6,606,675

Clock synchronization in systems with multi-channel high-speed bus subsystems

403 6,600,374

Collective automatic gain control

404 6,600,338

Apparatus and method for level-shifting input receiver circuit from high external voltage to low internal supply voltage

405 6,598,171

Integrated circuit I/O using a high performance bus interface

406 6,597,616

DRAM core refresh with reduced spike current

407 6,594,326

Apparatus and method for synchronizing a control signal

408 6,591,353

Protocol for communication with dynamic memory

409 6,590,781

Clock routing in multiple channel modules and bus systems

410 6,589,059

Chip socket assembly and chip file assembly for semiconductor chips

411 6,584,037

Memory device which samples data after an amount of time transpires

412 6,583,035

Semiconductor package with a controlled impedance bus and method of forming same

413 6,574,759

Method for verifying and improving run-time of a memory test

414 6,574,153

Asynchronous, high-bandwidth memory component using calibrated timing elements

415 6,573,779

Duty cycle integrator with tracking common mode feedback control

416 6,571,325

Pipelined memory controller and method of controlling access to memory devices in a memory system

417 6,570,944

Apparatus for data recovery in a synchronous chip-to-chip system

418 6,570,814

Integrated circuit device which outputs data after a latency period transpires

419 6,564,281

Synchronous memory device having automatic precharge

420 6,553,452

Synchronous memory device having a temperature register

421 6,552,948

Methods and systems for reducing heat flux in memory systems

422 6,546,446

Synchronous memory device having automatic precharge

423 6,546,343

Bus line current calibration

424 6,545,875

Multiple channel modules and bus systems using same

425 6,542,976

Memory device having an internal register

426 6,542,416

Methods and arrangements for conditionally enforcing CAS latencies in memory devices

427 6,539,072

Delay locked loop circuitry for clock delay adjustment

428 6,538,336

Wirebond assembly for high-speed integrated circuits

429 6,532,522

Asynchronous request/synchronous data dynamic random access memory

430 6,530,062

Active impedance compensation

431 6,523,089

Memory controller with power management logic

432 6,522,199

Reconfigurable dual-mode multiple stage operational amplifiers

433 6,516,365

Apparatus and method for topography dependent signaling

434 6,514,794

Redistributed bond pads in stacked integrated circuit die package

435 6,513,103

Method and apparatus for adjusting the performance of a synchronous memory system

436 6,513,081

Memory device which receives an external reference voltage signal

437 6,509,756

Method and apparatus for low capacitance, high output impedance driver

438 6,504,875

Apparatus for multilevel signaling

439 6,504,448

Apparatus and method for transmission line impedance tuning using periodic capacitive stubs

440 6,504,438

Dual loop phase lock loops using dual voltage supply regulators

441 6,504,405

Differential amplifier with selectable hysteresis and buffered filter

442 6,502,161

Memory system including a point-to-point linked memory subsystem

443 6,496,897

Semiconductor memory device which receives write masking information

444 6,496,889

Chip-to-chip communication system using an ac-coupled bus and devices employed in same

445 6,493,789

Memory device which receives write masking and automatic precharge information

446 6,480,035

Phase detector with minimized phase detection error

447 6,473,439

Method and apparatus for fail-safe resynchronization with minimum latency

448 6,470,405

Protocol for communication with dynamic memory

449 6,469,555

Apparatus and method for generating multiple clock signals from a single loop circuit

450 6,462,591

Semiconductor memory device having a controlled output driver characteristic

451 6,462,588

Asymmetry control for an output driver

452 6,453,401

Memory controller with timing constraint tracking and checking unit and corresponding method

453 6,452,863

Method of operating a memory device having a variable data input length

454 6,449,159

Semiconductor module with imbedded heat spreader

455 6,448,828

Apparatus and method for edge based duty cycle conversion

456 6,448,813

Output driver circuit with well-controlled output impedance

457 6,447,321

Socket for coupling an integrated circuit package to a printed circuit board

458 6,426,984

Apparatus and method for reducing clock signal phase skew in a master-slave system with multiple latent clock cycles

459 6,426,916

Memory device having a variable data output length and a programmable register

460 6,415,339

Memory device having a plurality of programmable internal registers and a delay time register

461 6,405,296

Asynchronous request/synchronous data dynamic random access memory

462 6,404,660

Semiconductor package with a controlled impedance bus and method of forming same

463 6,401,167

High performance cost optimized memory

464 6,396,887

Apparatus and method for generating a distributed clock signal using gear ratio techniques

465 6,396,329

Method and apparatus for receiving high speed signals with low latency

466 6,384,637

Differential amplifier with selectable hysteresis and buffered filter

467 6,378,020

System having double data transfer rate and intergrated circuit therefor

468 6,378,018

Memory device and system including a low power interface

469 6,376,904

Redistributed bond pads in stacked integrated circuit die package

470 6,373,768

Apparatus and method for thermal regulation in memory subsystems

471 6,373,293

Self-synchronized, multi-sample, quadrature phase detector

472 6,370,668

High speed memory system capable of selectively operating in non-chip-kill and chip-kill modes

473 6,369,652

Differential amplifiers with current and resistance compensation elements for balanced output

474 6,369,626

Low pass filter for a delay locked loop circuit

475 6,359,931

Apparatus and method for multilevel signaling

476 6,356,975

Apparatus and method for pipelined memory operations

477 6,352,435

Chip socket assembly and chip file assembly for semiconductor chips

478 6,349,050

Methods and systems for reducing heat flux in memory systems

479 6,347,354

Apparatus and method for maximizing information transfers over limited interconnect resources

480 6,345,009

Apparatus and method for refreshing subsets of memory devices in a memory system

481 6,343,352

Method and apparatus for two step memory write operations

482 6,343,042

DRAM core refresh with reduced spike current

483 6,342,800

Charge compensation control circuit and method for use with output driver

484 6,340,909

Method and apparatus for phase interpolation

485 6,340,900

Phase detector with minimized phase detection error

486 6,330,193

Method and apparatus for low capacitance, high output impedance driver

487 6,324,120

Memory device having a variable data output length

488 6,323,706

Apparatus and method for edge based duty cycle conversion

489 RE37,452

At frequency phase shifting circuit for use in a quadrature clock generator

490 6,321,282

Apparatus and method for topography dependent signaling

491 6,314,051

Memory device having write latency

492 6,310,814

Rambus DRAM (RDRAM) apparatus and method for performing refresh operations

493 6,308,232

Electronically moveable terminator and method for using same in a memory system

494 RE37,409

Memory and method for sensing sub-groups of memory elements

495 6,304,937

Method of operation of a memory controller

496 6,304,104

Method and apparatus for reducing worst case power

497 6,294,934

Current control technique

498 6,287,132

Connector with staggered contact design

499 6,282,604

Memory controller and method for meory devices with mutliple banks of memory cells

500 6,273,759

Multi-slot connector with integrated bus providing contact between adjacent modules

501 6,266,737

Method and apparatus for providing a memory with write enable information

502 6,266,730

High-frequency bus system

503 6,266,292

DRAM core refresh with reduced spike current

504 6,266,285

Method of operating a memory device having write latency

505 6,263,448

Power control system for synchronous memory device

506 6,260,097

Method and apparatus for controlling a synchronous memory device

507 6,234,820

Method and apparatus for joining printed circuit boards

508 6,232,796

Apparatus and method for detecting two data bits per clock edge

509 6,226,757

Apparatus and method for bus timing compensation

510 6,226,754

Apparatus and method for device timing compensation

511 6,209,071

Asynchronous request/synchronous data dynamic random access memory

512 6,205,191

Method and apparatus for synchronizing a control signal

513 6,204,697

Low-latency small-swing clocked receiver

514 6,198,307

Output driver circuit with well-controlled output impedance

515 6,185,644

Memory system including a plurality of memory devices and a transceiver device

516 6,182,184

Method of operating a memory device having a variable data input length

517 6,178,130

Apparatus and method for refreshing subsets of memory devices in a memory system

518 6,169,434

Conversion circuit with duty cycle correction for small swing signals, and associated method

519 6,163,178

Impedance controlled output driver

520 6,160,716

Motherboard having one-between trace connections for connectors

521 6,154,821

Method and apparatus for initializing dynamic random access memory (DRAM) devices by levelizing a read domain

522 6,151,239

Data packet with embedded mask

523 6,134,172

Apparatus for sharing sense amplifiers between memory banks

524 6,133,773

Variable delay element

525 6,128,696

Synchronous memory device utilizing request protocol and method of operation of same

526 6,125,422

Dependent bank memory controller method and apparatus

527 6,125,157

Delay-locked loop circuitry for clock delay adjustment

528 6,122,688

Protocol for communication with dynamic memory

529 6,122,208

Circuit and method for column redundancy for high bandwidth memories

530 6,122,189

Data packet with embedded mask

531 6,111,445

Phase interpolator with noise immunity

532 6,107,847

Zero power reset circuit for low voltage CMOS circuits

533 6,101,152

Method of operating a synchronous memory device

534 6,094,075

Current control technique

535 RE36,781

Differential comparator for amplifying small swing signals to a full swing output

536 6,085,284

Method of operating a memory device having a variable data output length and an identification register

537 6,075,744

Dram core refresh with reduced spike current

538 6,075,743

Method and apparatus for sharing sense amplifiers between memory banks

539 6,075,730

High performance cost optimized memory with delayed memory writes

540 6,070,222

Synchronous memory device having identification register

541 6,067,594

High frequency bus system

542 6,067,592

System having a synchronous memory device

543 6,049,846

Integrated circuit having memory which synchronously samples information with respect to external clock signals

544 6,047,346

System for adjusting slew rate on an output of a drive circuit by enabling a plurality of pre-drivers and a plurality of output drivers

545 6,044,426

Memory system having memory devices each including a programmable internal register

546 6,038,195

Synchronous memory device having a delay time register and method of operating same

547 6,035,369

Method and apparatus for providing a memory with write enable information

548 6,035,365

Dual clocked synchronous memory device having a delay time register and method of operating same

549 6,034,918

Method of operating a memory having a variable data output length and a programmable register

550 6,032,215

Synchronous memory device utilizing two external clocks

551 6,032,214

Method of operating a synchronous memory device having a variable data output length

552 6,021,076

Apparatus and method for thermal regulation in memory subsystems

553 6,014,042

Phase detector using switched capacitors

554 6,009,487

Method and apparatus for setting a current of an output driver for the high speed bus

555 6,007,357

Chip socket assembly and chip file assembly for semiconductor chips

556 6,005,895

Apparatus and method for multilevel signaling

557 6,002,589

Integrated circuit package for coupling to a printed circuit board

558 5,995,443

Synchronous memory device

559 5,995,016

Method and apparatus for N choose M device selection

560 5,983,320

Method and apparatus for externally configuring and modifying the transaction request response characteristics of a semiconductor device coupled to a bus

561 5,977,798

Low-latency small-swing clocked receiver

562 5,966,731

Protocol for communication with dynamic memory

563 5,959,481

Bus driver circuit including a slew rate indicator circuit having a one shot circuit

564 5,956,284

Method and apparatus for writing to memory components

565 5,954,804

Synchronous memory device having an internal register

566 5,953,263

Synchronous memory device having a programmable register and method of controlling same

567 5,945,862

Circuitry for the delay adjustment of a clock signal

568 5,940,340

Method and apparatus for writing to memory components

569 5,928,343

Memory module having memory devices containing internal device ID registers and method of initializing same

570 5,915,105

Integrated circuit I/O using a high performance bus interface

571 5,913,046

Protocol for communication with dynamic memory

572 5,908,333

Connector with integral transmission line bus

573 5,896,545

Transmitting memory requests for multiple block format memory operations the requests comprising count information, a mask, and a second mask

574 5,872,996

Method and apparatus for transmitting memory requests by transmitting portions of count data in adjacent words of a packet

575 RE36,013

Differential charge pump circuit with high differential and low common mode impedance

576 5,844,913

Current mode interface circuitry for an IC test device

577 5,844,855

Method and apparatus for writing to memory components

578 5,841,715

Integrated circuit I/O using high performance bus interface

579 5,841,580

Integrated circuit I/O using a high performance bus interface

580 5,825,209

Quadrature phase detector

581 5,809,263

Integrated circuit I/O using a high performance bus interface

582 5,808,498

At frequency phase shifting circuit for use in a quadrature clock generator

583 5,799,051

Delay stage circuitry for a ring oscillator

584 5,765,020

Method of transferring data by transmitting lower order and upper odermemory address bits in separate words with respective op codes and start information

585 5,764,963

Method and apparatus for performing maskable multiple color block writes

586 5,748,914

Protocol for communication with dynamic memory

587 5,748,554

Memory and method for sensing sub-groups of memory elements

588 5,736,892

Differential charge pump circuit with high differential impedance and low common mode impedance

589 5,715,407

Process and apparatus for collision detection on a parallel bus by monitoring a first line of the bus during even bus cycles for indications of overlapping packets

590 5,680,361

Method and apparatus for writing to memory components

591 5,663,661

Modular bus with single or double parallel termination

592 5,657,481

Memory device with a phase locked loop circuitry

593 5,638,334

Integrated circuit I/O using a high performance bus interface

594 5,621,340

Differential comparator for amplifying small swing signals to a full swing output

595 5,614,855

Delay-locked loop

596 5,606,717

Memory circuitry having bus interface for receiving information in packets and access time registers

597 5,596,610

Delay stage circuitry for a ring oscillator

598 5,578,940

Modular bus with single or double parallel termination

599 5,572,158

Amplifier with active duty cycle correction

600 5,554,945

Voltage controlled phase shifter with unlimited range

601 5,537,573

Cache system and method for prefetching of data

602 5,513,327

Integrated circuit I/O using a high performance bus interface

603 5,511,024

Dynamic random access memory system

604 5,499,385

Method for accessing and transmitting data to/from a memory in packets

605 5,499,355

Prefetching into a cache to minimize main memory access time and cache size in a computer system

606 5,488,321

Static high speed comparator

607 5,485,490

Method and circuitry for clock synchronization

608 5,473,575

Integrated circuit I/O using a high performance bus interface

609 5,451,898

Bias circuit and differential amplifier having stabilized output swing

610 5,446,696

Method and apparatus for implementing refresh in a synchronous DRAM system

611 5,434,817

Dynamic random access memory system

612 5,432,823

Method and circuitry for minimizing clock-data skew in a bus system

613 5,430,676

Dynamic random access memory system

614 5,422,529

Differential charge pump circuit with high differential and low common mode impedance

615 5,408,129

Integrated circuit I/O using a high performance bus interface

616 5,390,308

Method and apparatus for address mapping of dynamic random access memory

617 5,357,195

Testing set up and hold input timing parameters of high speed integrated circuit devices

618 5,355,391

High speed bus system

619 5,337,285

Method and apparatus for power control in devices

620 5,325,053

Apparatus for testing timing parameters of high speed integrated circuit devices

621 5,319,755

Integrated circuit I/O using high performance bus interface

622 5,268,639

Testing timing parameters of high speed integrated circuit devices

623 5,254,883

Electrical current source circuitry for a bus

624 5,243,703

Apparatus for synchronously generating clock signals in a data processing system