

List of 624 patents owned by Rambus, compiled by sabatino Dec 26 2008

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Methods and apparatus for bi-directional signaling

401 6,608,507

Memory system including a memory device having a controlled output driver characteristic

402 6,606,675

Clock synchronization in systems with multi-channel high-speed bus subsystems

403 6,600,374

Collective automatic gain control

404 6,600,338

Apparatus and method for level-shifting input receiver circuit from high external voltage to low internal supply voltage

405 6,598,171

Integrated circuit I/O using a high performance bus interface

406 6,597,616

DRAM core refresh with reduced spike current

407 6,594,326

Apparatus and method for synchronizing a control signal

408 6,591,353

Protocol for communication with dynamic memory

409 6,590,781

Clock routing in multiple channel modules and bus systems

410 6,589,059

Chip socket assembly and chip file assembly for semiconductor chips

411 6,584,037

Memory device which samples data after an amount of time transpires

412 6,583,035

Semiconductor package with a controlled impedance bus and method of forming same

413 6,574,759

Method for verifying and improving run-time of a memory test

414 6,574,153

Asynchronous, high-bandwidth memory component using calibrated timing elements

415 6,573,779

Duty cycle integrator with tracking common mode feedback control

416 6,571,325

Pipelined memory controller and method of controlling access to memory devices in a memory system

417 6,570,944

Apparatus for data recovery in a synchronous chip-to-chip system

418 6,570,814

Integrated circuit device which outputs data after a latency period transpires

419 6,564,281

Synchronous memory device having automatic precharge

420 6,553,452

Synchronous memory device having a temperature register

421 6,552,948

Methods and systems for reducing heat flux in memory systems

422 6,546,446

Synchronous memory device having automatic precharge

423 6,546,343

Bus line current calibration

424 6,545,875

Multiple channel modules and bus systems using same

425 6,542,976

Memory device having an internal register

426 6,542,416

Methods and arrangements for conditionally enforcing CAS latencies in memory devices

427 6,539,072

Delay locked loop circuitry for clock delay adjustment

428 6,538,336

Wirebond assembly for high-speed integrated circuits

429 6,532,522

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430 6,530,062

Active impedance compensation

431 6,523,089

Memory controller with power management logic

432 6,522,199

Reconfigurable dual-mode multiple stage operational amplifiers

433 6,516,365

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434 6,514,794

Redistributed bond pads in stacked integrated circuit die package

435 6,513,103

Method and apparatus for adjusting the performance of a synchronous memory system

436 6,513,081

Memory device which receives an external reference voltage signal

437 6,509,756

Method and apparatus for low capacitance, high output impedance driver

438 6,504,875

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439 6,504,448

Apparatus and method for transmission line impedance tuning using periodic capacitive stubs

440 6,504,438

Dual loop phase lock loops using dual voltage supply regulators

441 6,504,405

Differential amplifier with selectable hysteresis and buffered filter

442 6,502,161

Memory system including a point-to-point linked memory subsystem

443 6,496,897

Semiconductor memory device which receives write masking information

444 6,496,889

Chip-to-chip communication system using an ac-coupled bus and devices employed in same

445 6,493,789

Memory device which receives write masking and automatic precharge information

446 6,480,035

Phase detector with minimized phase detection error

447 6,473,439

Method and apparatus for fail-safe resynchronization with minimum latency

448 6,470,405

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449 6,469,555

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450 6,462,591

Semiconductor memory device having a controlled output driver characteristic

451 6,462,588

Asymmetry control for an output driver

452 6,453,401

Memory controller with timing constraint tracking and checking unit and corresponding method

453 6,452,863

Method of operating a memory device having a variable data input length

454 6,449,159

Semiconductor module with imbedded heat spreader

455 6,448,828

Apparatus and method for edge based duty cycle conversion

456 6,448,813

Output driver circuit with well-controlled output impedance

457 6,447,321

Socket for coupling an integrated circuit package to a printed circuit board

458 6,426,984

Apparatus and method for reducing clock signal phase skew in a master-slave system with multiple latent clock cycles

459 6,426,916

Memory device having a variable data output length and a programmable register

460 6,415,339

Memory device having a plurality of programmable internal registers and a delay time register



461 6,405,296

Asynchronous request/synchronous data dynamic random access memory

462 6,404,660

Semiconductor package with a controlled impedance bus and method of forming same

463 6,401,167

High performance cost optimized memory

464 6,396,887

Apparatus and method for generating a distributed clock signal using gear ratio techniques

465 6,396,329

Method and apparatus for receiving high speed signals with low latency

466 6,384,637

Differential amplifier with selectable hysteresis and buffered filter

467 6,378,020

System having double data transfer rate and intergrated circuit therefor

468 6,378,018

Memory device and system including a low power interface

469 6,376,904

Redistributed bond pads in stacked integrated circuit die package

470 6,373,768

Apparatus and method for thermal regulation in memory subsystems

471 6,373,293

Self-synchronized, multi-sample, quadrature phase detector

472 6,370,668

High speed memory system capable of selectively operating in non-chip-kill and chip-kill modes

473 6,369,652

Differential amplifiers with current and resistance compensation elements for balanced output

474 6,369,626

Low pass filter for a delay locked loop circuit

475 6,359,931

Apparatus and method for multilevel signaling

476 6,356,975

Apparatus and method for pipelined memory operations

477 6,352,435

Chip socket assembly and chip file assembly for semiconductor chips

478 6,349,050

Methods and systems for reducing heat flux in memory systems

479 6,347,354

Apparatus and method for maximizing information transfers over limited interconnect resources

480 6,345,009

Apparatus and method for refreshing subsets of memory devices in a memory system

481 6,343,352

Method and apparatus for two step memory write operations

482 6,343,042

DRAM core refresh with reduced spike current

483 6,342,800

Charge compensation control circuit and method for use with output driver

484 6,340,909

Method and apparatus for phase interpolation

485 6,340,900

Phase detector with minimized phase detection error

486 6,330,193

Method and apparatus for low capacitance, high output impedance driver

487 6,324,120

Memory device having a variable data output length

488 6,323,706

Apparatus and method for edge based duty cycle conversion

489 RE37,452

At frequency phase shifting circuit for use in a quadrature clock generator

490 6,321,282

Apparatus and method for topography dependent signaling

491 6,314,051

Memory device having write latency

492 6,310,814

Rambus DRAM (RDRAM) apparatus and method for performing refresh operations

493 6,308,232

Electronically moveable terminator and method for using same in a memory system

494 RE37,409

Memory and method for sensing sub-groups of memory elements

495 6,304,937

Method of operation of a memory controller

496 6,304,104

Method and apparatus for reducing worst case power

497 6,294,934

Current control technique

498 6,287,132

Connector with staggered contact design

499 6,282,604

Memory controller and method for memory devices with multiple banks of memory cells

500 6,273,759

Multi-slot connector with integrated bus providing contact between adjacent modules

501 6,266,737

Method and apparatus for providing a memory with write enable information

502 6,266,730

High-frequency bus system

503 6,266,292

DRAM core refresh with reduced spike current

504 6,266,285

Method of operating a memory device having write latency

505 6,263,448

Power control system for synchronous memory device

506 6,260,097

Method and apparatus for controlling a synchronous memory device

507 6,234,820

Method and apparatus for joining printed circuit boards

508 6,232,796

Apparatus and method for detecting two data bits per clock edge

509 6,226,757

Apparatus and method for bus timing compensation

510 6,226,754

Apparatus and method for device timing compensation

511 6,209,071

Asynchronous request/synchronous data dynamic random access memory

512 6,205,191

Method and apparatus for synchronizing a control signal

513 6,204,697

Low-latency small-swing clocked receiver

514 6,198,307

Output driver circuit with well-controlled output impedance

515 6,185,644

Memory system including a plurality of memory devices and a transceiver device

516 6,182,184

Method of operating a memory device having a variable data input length

517 6,178,130

Apparatus and method for refreshing subsets of memory devices in a memory system

518 6,169,434

Conversion circuit with duty cycle correction for small swing signals, and associated method

519 6,163,178

Impedance controlled output driver

520 6,160,716

Motherboard having one-between trace connections for connectors

521 6,154,821

Method and apparatus for initializing dynamic random access memory (DRAM) devices by levelizing a read domain

522 6,151,239

Data packet with embedded mask

523 6,134,172

Apparatus for sharing sense amplifiers between memory banks

524 6,133,773

Variable delay element

525 6,128,696

Synchronous memory device utilizing request protocol and method of operation of same

526 6,125,422

Dependent bank memory controller method and apparatus

527 6,125,157

Delay-locked loop circuitry for clock delay adjustment

528 6,122,688

Protocol for communication with dynamic memory

529 6,122,208

Circuit and method for column redundancy for high bandwidth memories

530 6,122,189

Data packet with embedded mask

531 6,111,445

Phase interpolator with noise immunity

532 6,107,847

Zero power reset circuit for low voltage CMOS circuits

533 6,101,152

Method of operating a synchronous memory device

534 6,094,075

Current control technique

535 RE36,781

Differential comparator for amplifying small swing signals to a full swing output

536 6,085,284

Method of operating a memory device having a variable data output length and an identification register

537 6,075,744

Dram core refresh with reduced spike current

538 6,075,743

Method and apparatus for sharing sense amplifiers between memory banks

539 6,075,730

High performance cost optimized memory with delayed memory writes

540 6,070,222

Synchronous memory device having identification register

541 6,067,594

High frequency bus system

542 6,067,592

System having a synchronous memory device

543 6,049,846

Integrated circuit having memory which synchronously samples information with respect to external clock signals

544 6,047,346

System for adjusting slew rate on an output of a drive circuit by enabling a plurality of pre-drivers and a plurality of output drivers

545 6,044,426

Memory system having memory devices each including a programmable internal register

546 6,038,195

Synchronous memory device having a delay time register and method of operating same

547 6,035,369

Method and apparatus for providing a memory with write enable information

548 6,035,365

Dual clocked synchronous memory device having a delay time register and method of operating same

549 6,034,918

Method of operating a memory having a variable data output length and a programmable register

550 6,032,215

Synchronous memory device utilizing two external clocks

551 6,032,214

Method of operating a synchronous memory device having a variable data output length

552 6,021,076

Apparatus and method for thermal regulation in memory subsystems

553 6,014,042

Phase detector using switched capacitors

554 6,009,487

Method and apparatus for setting a current of an output driver for the high speed bus

555 6,007,357

Chip socket assembly and chip file assembly for semiconductor chips

556 6,005,895

Apparatus and method for multilevel signaling

557 6,002,589

Integrated circuit package for coupling to a printed circuit board

558 5,995,443

Synchronous memory device

559 5,995,016

Method and apparatus for N choose M device selection

560 5,983,320

Method and apparatus for externally configuring and modifying the transaction request response characteristics of a semiconductor device coupled to a bus

561 5,977,798

Low-latency small-swing clocked receiver

562 5,966,731

Protocol for communication with dynamic memory

563 5,959,481

Bus driver circuit including a slew rate indicator circuit having a one shot circuit

564 5,956,284

Method and apparatus for writing to memory components

565 5,954,804

Synchronous memory device having an internal register

566 5,953,263

Synchronous memory device having a programmable register and method of controlling same

567 5,945,862

Circuitry for the delay adjustment of a clock signal

568 5,940,340

Method and apparatus for writing to memory components

569 5,928,343

Memory module having memory devices containing internal device ID registers and method of initializing same

570 5,915,105

Integrated circuit I/O using a high performance bus interface

571 5,913,046

Protocol for communication with dynamic memory

572 5,908,333

Connector with integral transmission line bus

573 5,896,545

Transmitting memory requests for multiple block format memory operations the requests comprising count information, a mask, and a second mask

574 5,872,996

Method and apparatus for transmitting memory requests by transmitting portions of count data in adjacent words of a packet

575 RE36,013

Differential charge pump circuit with high differential and low common mode impedance

576 5,844,913



Current mode interface circuitry for an IC test device

577 5,844,855

Method and apparatus for writing to memory components

578 5,841,715

Integrated circuit I/O using high performance bus interface

579 5,841,580

Integrated circuit I/O using a high performance bus interface

580 5,825,209

Quadrature phase detector

581 5,809,263

Integrated circuit I/O using a high performance bus interface

582 5,808,498

At frequency phase shifting circuit for use in a quadrature clock generator

583 5,799,051

Delay stage circuitry for a ring oscillator

584 5,765,020

Method of transferring data by transmitting lower order and upper order memory address bits in separate words with respective op codes and start information

585 5,764,963

Method and apparatus for performing maskable multiple color block writes

586 5,748,914

Protocol for communication with dynamic memory

587 5,748,554

Memory and method for sensing sub-groups of memory elements

588 5,736,892

Differential charge pump circuit with high differential impedance and low common mode impedance

589 5,715,407

Process and apparatus for collision detection on a parallel bus by monitoring a first line of the bus during even bus cycles for indications of overlapping packets

590 5,680,361

Method and apparatus for writing to memory components

591 5,663,661

Modular bus with single or double parallel termination

592 5,657,481

Memory device with a phase locked loop circuitry

593 5,638,334

Integrated circuit I/O using a high performance bus interface

594 5,621,340

Differential comparator for amplifying small swing signals to a full swing output

595 5,614,855

Delay-locked loop

596 5,606,717

Memory circuitry having bus interface for receiving information in packets and access time registers

597 5,596,610

Delay stage circuitry for a ring oscillator

598 5,578,940

Modular bus with single or double parallel termination

599 5,572,158

Amplifier with active duty cycle correction

600 5,554,945

Voltage controlled phase shifter with unlimited range

601 5,537,573

Cache system and method for prefetching of data

602 5,513,327

Integrated circuit I/O using a high performance bus interface

603 5,511,024

Dynamic random access memory system

604 5,499,385

Method for accessing and transmitting data to/from a memory in packets

605 5,499,355

Prefetching into a cache to minimize main memory access time and cache size in a computer system

606 5,488,321

Static high speed comparator

607 5,485,490

Method and circuitry for clock synchronization

608 5,473,575

Integrated circuit I/O using a high performance bus interface

609 5,451,898

Bias circuit and differential amplifier having stabilized output swing

610 5,446,696

Method and apparatus for implementing refresh in a synchronous DRAM system

611 5,434,817

Dynamic random access memory system

612 5,432,823

Method and circuitry for minimizing clock-data skew in a bus system

613 5,430,676

Dynamic random access memory system

614 5,422,529

Differential charge pump circuit with high differential and low common mode impedance

615 5,408,129

Integrated circuit I/O using a high performance bus interface

616 5,390,308

Method and apparatus for address mapping of dynamic random access memory

617 5,357,195

Testing set up and hold input timing parameters of high speed integrated circuit devices

618 5,355,391

High speed bus system

619 5,337,285

Method and apparatus for power control in devices

620 5,325,053

Apparatus for testing timing parameters of high speed integrated circuit devices

621 5,319,755

Integrated circuit I/O using high performance bus interface

622 5,268,639

Testing timing parameters of high speed integrated circuit devices

623 5,254,883

Electrical current source circuitry for a bus

624 5,243,703

Apparatus for synchronously generating clock signals in a data processing system