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IDEM JOB 03-03-011

CERTIFICATION OF ACCURACY

I CERTIFY, UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE UNITED STATES OF AMERICA THAT WE ARE COMPETENT IN ENGLISH AND **JAPANESE** AND THAT THE FOLLOWING WITH **BATES NUMBERS MEC000328 THRU MEC000335, MEC001441 AND MEC001748** ARE, TO THE BEST OF OUR KNOWLEDGE AND BELIEF, TRUE, CORRECT, COMPLETE AND ACCURATE TRANSLATIONS OF THE ORIGINAL AND ATTACHED JAPANESE DOCUMENTS WITH THE SAME BATES NUMBERS AS MENTIONED ABOVE.

MARCH 17, 2003

MARIAM NAYINY
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To: Nagasawa FM

Evaluation of Rambus Patent Agreement
July 1993[?]
System Development Computers
[Seal: [Illeg.] [Illeg.] 7/13/93]
Memo I J [Seal: Matsumoto Memo I J 7/13/93]

1. Purpose of this memo

Several years ago, Rambus Inc. approached us about its so-called Rambus patent, which could presumably be used in building an ultra high-speed memory system.

We were skeptical about said technology's feasibility and broad acceptance in the market place, and therefore, we decided to continuously watch this technology but not to actively contact the company. Instead, we have been proceeding with a policy of focusing on CDRAM, which had been announced by our company and had been ahead of Rambus in the field. Additionally, Rambus Inc.s' presentation did not clearly indicate what was new.

However, as we learned that our competitors had recognized the importance of said patent and signed agreements, we searched for patents that had been applied for (PCT International Application) and examined the content of Rambus patent with cooperation from UL Lab, SL Lab (LS Lab/CL Lab), as well as Koden and Jodenken. Based on this investigation, we will decide again whether it is necessary to sign an agreement. In investigating the patent, rather than examining each and every prior art for individual claims, we tried to focus on determining the usefulness of the patent from a technical viewpoint by assuming that the patent is valid.

2. Rambus Inc.s' contract conditions and statuses at other companies

1) Contract conditions

Recently, approximately 700 million yen (initial payment) + Running royalty of 2%. Will be more expensive after commercialization. Once an agreement is signed, there is an obligation to proceed with the development of LSI. This obligation is placed only on LSI manufacturers. Free disclosure to LSI users.

2) Statuses at Japanese competitors

Toshiba ... Already signed an agreement. Already prototyped a 4M Rambus dram (RDRAM).

NEC ... Already signed an agreement. Designing a 16M RDRAM (prototype within this year). It appears that an NEC User Division is evaluating an application to images.

Fujitsu ... Already signed an agreement. Appears to be evaluating a Rambus ASIC.

Hitachi ... Already signed an agreement. Found the patent and decided it was important. Hitachi must have successfully altered the "contract conditions" because it has been said that Hitachi will not make RDRAM itself.

3. Major user trend

HP ... Not interested
DEC ... Not interested
SUN ... Not interested
SGI ... There is a rumor that SGI is considering RDRAM for images, in addition to SDRAM and CDRAM.

4. Features/key points of Rambus technology (claimed by Rambus Inc.)

- A data transfer speed of 500 M bytes/sec (with a clock cycle of 2 ns) can be obtained from each RDRAM on a narrow bus that has 16 active signals.
- If multiple Rambus channels are used, applications with even higher bandwidths are possible.
- Can be implemented using standard CMOS process/PCB material.

• Since chips are directly connected, glue chips or buffers are not necessary at all.
Note: This claim is highly questionable. At least until a dedicated MPU is developed, a bridge LSI will be required.
• Significantly improves the price-performance ratio of the main memory system of high-performance 32/64 bit microprocessors.
• Cheaper than VRAM and a maximum of 3 to 5 times the performance improvement over a VRAM-based system.
• Because the sense amplifier inside each RDRAM is used as a high-speed cache, a data transmission/receiving at 500 M bytes/sec is possible.
• Because each RDRAM has two independent banks, the hit rate is improved and the average latency is reduced.
• Innovative, low-voltage, impedance-controlled signals enable 500 M bytes/sec operation.
Etc.

5. Rambus patent

1) Title: Integrated Circuit I/O Using A High Performance Bus System
International Publication Number: WO 91/166680
International Publication Date: October 31, 1991
International Filing Date: April 16, 1991
Priority Data: 510898: April 18, 1990

2) Configuration: Number of claims: 150 (independent claims: 21), consists of 135 pages.
3) Claims
a. Bus description (Claims 1 through 12)
Claim 1: Memory subsystem comprising
• two memory devices connected in parallel to a bus,
• said bus including a plurality of (a pair of) bus lines for carrying substantially all addresses, data and control information needed by (two) memory devices,
• said control information including device-select information,
• said bus containing substantially fewer bus lines than the number of bits necessary for specifying a pair of addresses, and
• said bus carrying device-select information without the need for separate device-select lines connected directly to individual memory devices.

This is the basis of the Rambus patent, and many of the claims described below are based on this claim (or its modified versions) and expand into a system and LSI for implementing it.

b. Register group description (Claims 13 through 24)
Describes various types of registers provided in an LSI on the bus that is based on Claim 1, and its functions, etc.

c. Transaction (job switching and processing), request pocket, and protocol description (Claims 25 through 67)
Describes the transactions, inter-device request pockets, and communication protocol that are activated by the master device, based on Claim 1.

d. Clock description (Claims 68 through 81)
Claims a system clock format, an input method, and a method of generating an internal LSI clock synchronously with said clock based on Claim 1. The important point is the following:
• A bus subsystem comprising a semiconductor device containing a clock generator that ...

... determines (seeks) the mid-point between a clock signal with an earlier phase and a clock signal with a delayed phase (which run on the clock supply lines that travel in both directions on the bus), and that generates an internal LSI clock that is synchronized with said mid-point.

With this method, it is possible to supply absolutely synchronized clock signals to all LSIs on the bus regardless of the delays due to signal routes.

e. DRAM description (Claims 82 through 90)
Describes the characteristics that DRAM on this bus must possess.

f. Package description (Claims 91 through 94)

g. and beyond. Describes the aforementioned claims more specifically. (Claims 95 through 150)

6. Evaluation
The Patent Specification was discussed and evaluated by the following people several times:
Memo I: Matsumoto J; Technology Development: Sasahara K; System Development: Shimonishi TB; UL Lab L
New RAM: Dosaka T; SL Lab Design Technology I: Asahina T

The following two points were considered to be most important:

1) Bus description under a. in Section 5-3) above
A method that (can) reduce bus width is nothing new. Furthermore, as summarized in Appendix 1, the examiner of the International Search Report has also cited a prior art.
However, since this description is the basis of the patent, we decided to ask Koden and Jodenken about user opinions on future trends in particular. Furthermore, even though this description is the basis of the patent, it is quite predictable that [Rambus] will try to establish a patent that is separate from said bus by narrowing the scope in case of a rejection.

2) Description of the clock in d. in Section 5-3) above
Although a prior art is cited for this item as well (Appendix 1), it is not exactly the same.

Claims 66 through 72
- all of the bus data lines (on the bus) comprising terminated propagation lines, and all information comprising a continuous bit string of small-amplitude signals,
- an LSI having a current mode driver being connected to said bus line,
- each LSI on the bus having a means of detecting whether or not other (none, one, or at least one) LSIs on the bus are driving their current mode drivers, based on the changes (in amplitude) in the small-amplitude signals,
- each LSI on the bus having multiple input circuits connected to individual data lines, and having a means of selecting an input circuit in order to detect and store individual bits consisting of continuous bit strings.

This is a DC-like description.

Claims 73 through 78 (The following is considered important. See Appendix 2.)
- The bus subsystem is configured as shown in Appendix 2. As for the clock in particular, a clock generator is provided on one (left) end, and a clock with an earlier phase is generated at the normal rising edge and is then turned around at the other (right) edge, and a clock with an earlier phase is returned to the left edge as a clock with a delayed phase. Each LSI on the bus can detect both the clock with an earlier phase and the clock with a delayed phase.
- Each LSI on the bus has a clock generator that determines (seeks) the mid-point between the aforementioned clock with an earlier phase and the clock with a delayed phase, and that generates an internal LSI clock that is synchronized with said mid-point.

Note: As shown in the figure on the bottom of Appendix 2, the aforementioned mid-point supplies absolutely synchronized time to CPUs, ROM, and DRAM (regardless of their locations). This concept is considered important.

Claims 79 through 81

• A concept of a (low-skew) clock generator that generates an internal LSI clock that is synchronized with said mid-point. (Appendixes 3 and 4)

The clock (CLK1, 53/100) with an earlier phase and the clock (CLK2, 54/100) with a delayed phase having small-amplitudes are converted into full-swing signals by a DC amplifier (102) (This may not be necessary for CLK2. Although the amplifier for CLK2 is not shown in the figure, this can be easily corrected in the patent.),

Amplified CLK1 is connected to a variable delay line (103) having a first variable time (X_0), the aforementioned output is connected to three delay lines (#1, 104; #2, 105; and #3, 106),

delay line #1 having a fixed delay time (t_0),

delay line #2 having a fixed delay time (t_0) + second variable time (X),

delay line #3 having a fixed delay time (t_0) + (X/2),

a clocked receiver (101) for receiving CLK1 being set to "active" by the output (107) of delay line #1, wherein

a means (filter 1, indicated by 116) is provided that can adjust the delay time of the variable delay line (103) so as to sample CLK1 during its transition,

a clocked receiver (111) for receiving CLK2 being set to "active" by the output (108) of delay line #2, wherein

a means (filter 2, indicated by 115) is provided that can adjust the delay time of the variable delay line (105) so as to sample CLK2 during its transition,

wherein the output (73) of delay line #3 being synchronized to the mid-point between the output (107) of delay line #1 and the output (108) of delay line #2 and being used as an internal LSI clock.

• the aforementioned first low-skew clock signal generation circuits which generate a "true" internal LSI clock, and the aforementioned second low-skew clock signal generation circuits generate a "complement" internal LSI clock which is opposite in logical value to said "true" clock.

Specific explanations follow.

• CLK1 - 107 generate a low-skew clock 107, which is well-synchronized to CLK1. Now, it is assumed that 0 < X_0 + t_0 < T. Although t_0 = 0 would be OK, the delays in 100 through 103 would directly manifest as being large (high sensitivity) with various fluctuations in that case. Therefore, a fixed t_0 value is added. The output 107 of delay line (circuit) #1 is fed back to 101, and Filter 1 (a phase-detector PLL will actually be used) supplies a signal (voltage) for controlling the delay volume X_0 to the delay line (delay circuit) 103. The t_0 generation circuit can be called a delay PLL. These are known technologies.

• Delay line (circuit) #2 generates the input time difference X between CLK1 and CLK2 as a low-skew clock. Filter 2 is a PLL for detecting the phases of 108 and 111, and its output 115 controls the delay volume X so that there is no jittering.

• Delay line (circuit) #3 generates 1/2 the input time difference X between CLK1 and CLK2, ...

...and generates an internal LSI clock 73[?], which is synchronized to the mid-point between CLK1 and CLK2. This volume (X/2) is generated in an analog or digital mode based on the output 115 of Filter 2. It is possible to think of a digital circuit that generates a low-skew clock 73[?] for each input time difference K between CLK1 and CLK2 by selecting the output 115 of Filter 2 as the stage number of an inverter by means of a selector and via an A/D converter.

* The following points are considered novel:

i) The input time difference X between CLK1 and CLK2 is converted into the control voltage 115 and a clock that is delayed by X/2 from CLK1 is generated by the control voltage 115, and therefore, operations without any adjustments are possible when the time difference between CLK1 and CLK2 is smaller than T_{CLK1} (= 1/f $_{CLK1}$).

ii) A possible shortcoming of this method is as follows. Because the output of the phase lock circuit (PLL) for locking the phase to CLK1, which consists of 101, 102, 103, and Filter 1, becomes the input for the second phase lock circuit (PLL) for locking the phase to CLK2, which consists of 111, 105, and Filter 2, there is a risk that the normal errors (jitters) during the locking of first/second PLL may both affect the output clock 73.

iii) The first PLL for locking the phase to CLK1 is highly stable because the change in the control signal 116 relative to the change in the delay time X_0 of the variable delay line 103 [i.e., $\delta X_0/\delta Y_{116}$] can be reduced by appropriately selecting the fixed delay time (t_0). However, the second PLL for locking the phase to CLK2 is considered difficult to implement using circuits because the time difference between CLK1 and CLK2 falls between 0 and T_{CLK1}, making the value of $\delta X/\delta Y_{115}$ greater than that for the first PLL circuit.

iv) As is described in the Specification of the patent, (because the input time difference between CLK1 and CLK2 is restricted to a value between 0 and T_{CLK1}) Rambus' physical line length is limited to approximately 8 cm in order to maximize performance. Therefore, the number of LSIs on the bus will also be limited. Rambus claims that this limitation can be eliminated by providing bridge LSIs. In other words, nothing is impossible according to Rambus.

7. Opinions of Koden/Jodenken

We had previously obtained the system-side opinions on Rambus Inc.s' presentation from Koden/Jodenken. See Appendix 5.

Since then, said patent Specification was found. Therefore, we again asked about the significance [of the patent] from a user's viewpoint based on the evaluation done by Hokuden/UL Lab/SL Lab.

Items evaluated with special attention

1) When future systems are considered, it will not be possible to keep increasing bus width. Therefore, will this method (a narrow bus width and protocol-based communication) become essential? Are there any other possible approaches?

2) If this approach is essential, is this patent itself a threat? What is the possibility that this patent will be granted? Are there any countermeasures?

3) A patent application has been filed for a method of synchronizing the absolute timing of multiple devices on a bus in order to achieve stable high-speed operation. Is such a method practical (feasible)?

Opinions of Koden/Jodenken (Summary was provided by Sakao BS of Koden. See Appendix 6 for details.)

1) Decreasing the bus width is one of the directions in the industry. However, individual technologies such as "decreasing the bus width" and "communication based on protocol" have already been in use.

2) Aside from the question of whether these individual technologies infringe on the Rambus patent, they will continue to be used in the future. There is a possibility that the Rambus patent itself will be granted in a limited scope.
However, in order for the technology to become widespread, major microprocessor makers, such as Intel, will have to develop processors that support Rambus. However, no such move is currently seen at Intel. Rather, there is a rumor that Intel might use the GTL interface starting with P6.

3) Since future DRAM will move toward a synchronous type and the burst mode, this idea, which can eliminate clock skew, is thought to be original.

4) Since there is a method that reduces or distributes requests to a bus by means of cache size increase, memory interpreter, etc., Rambus is not considered to be the only solution.

5) Given 2) and 4) above, Koden/Jodenken are currently not considering the adoption [of Rambus].

8. Conclusion

Although it is not easy to draw a conclusion from the above evaluation, we will take the following approach by taking our policy into consideration as well:

1) We will not take any immediate action, such as signing an agreement, and will continue watching technical trends as before.

2) As for the DRAM portion of the patent, various kinds of DRAM are being developed based on the specifications of DRAM on the Rambus. However, since Rambus might try to establish a patent that is separate from a bus by narrowing the scope in case the application for Rambus itself is rejected, those people involved in DRAM will continue to evaluate its usefulness and carry out prior art investigation in detail.

3) As for the concept of a low-skew clock generator, the prior art cited in the International Search Report will be examined in greater detail to verify the validity of the prior art.

Reasons and Discussions
1) The direction of narrower bus width and higher speed will continue to exist in the future. It might even accelerate. However, Rambus is not the only solution.

2) On the other hand, the bus width of microprocessors (MPUs) is expanding from 32 to 64 bits, and it is doubtful that new 8-bit versions will be developed now. However, products containing an 8-bit conversion circuit might be developed. Even if such products are developed, a clock speed of 250 to 500 MHz (depending on cycle control or edge control) will be needed for the MPU in order to take full advantage of this bus.

3) A possible method, as is described in a Rambus application note, is to insert a bridge LSI between the MPU and the devices on the bus. A 32-bit machine will execute a single instruction in four Rambus cycles (8 ns). The high-speed performance of the bus cannot necessarily be achieved with a 66-MHz internal/33-MHz interface MPU (30 ns). If there is an MPU with a 125-MHz interface (8 ns, 250-MHz internal), it can execute processes with no wait. This frequency can be loosened by 1/2 for a 64-bit machine. If two pairs of buses are provided, 250 MHz/125 MHz MPU can be used without any losses.

4) We have been carrying out various types of comparisons and evaluations regarding the application of the aforementioned [Rambus] to the main memory. However, because the cache line size is generally not very large, a large latency will cause the overall performance to be about the same as that of SDRAM/CDRAM or worse than that of CDRAM in some cases in our opinion. Furthermore, given the fact that the aforementioned MPU and bridge LSI are bus-specific and the fact that the RDRAM price will be high even without including a licensing fee (Rambus Inc. itself agrees with these points), [Rambus] is not likely to spread to applications that require large memory sizes. We have recently encountered a case in which a customer would not agree to a cost increase of several percentage points for the main memory.

5) Because of the reasons stated in 2) and 4), neither main users nor general users are likely to move to adopt [Rambus].

6) Rambus Inc. itself has said that PC makers' interest level is currently (as of June '93) low. However, the company said the interest level of makers involved in image processing is high. (SGI used to be extremely aggressive, but as explained in Section 3, the company seems to be evaluating SDRAM and CDRAM on the same level.)

7) According to Rambus Inc.'s demonstration, 200-MHz clock is propagated beautifully using a 4-layer glass epoxy substrate. Points 5) and 6) were supplied by Hamano FCH of [Illeg.] Semiconductor Technology.

8) Since [Rambus] can serially transfer 256 bytes at a rate of 500 MB/sec, it is suitable for burst-mode image processing. Especially, with significant advances in the Windows, moving/enlarging/shrinking of windows and bit-bit cutting (block transfer) control many of the applications, and performance improvement over VRAM is quite advantageous. Furthermore, because many of the filling algorithms are carried out based on scanning in the X-direction, high-speed processing becomes possible. In line-drawing in the Y direction, RDRAM must always return to the precharge state and thus has no performance advantage over VRAM. Even in bit-bit/filling operations, there are naturally cycles in which RDRAM must return to the precharge state. However, the precharge cycle can be ignored because of the high-speed scanning performance in the X direction. This is the reason why makers involved in image processing are interested in [RDRAM]. We are also concerned about this point.

9) A DEC engineer said that the fact that [RDRAM] does not offer any advantage in line-drawing operation in the aforementioned Y direction is the biggest shortcoming.

10) There is a possibility that the concept of low-skew clock generator described in detail in Section 6 will affect system LSIs that integrate CPUs and memory, as a system patent and not as a Rambus or MCM [patent]. We have heard of a competitor who signed an agreement with [Rambus Inc.], not because of Rambus but because of the perceived importance of this concept. However, the line length is limited to about 10 mm inside a chip, and the time difference between a clock with an earlier phase and a clock with a delayed phase is between 100 and 200 ps, which cannot be considered useful in actual applications.

11) At the current point in time, it is highly doubtful that Rambus will be widely adopted in the industry. On the other hand, it might become popular. Nonetheless, Rambus is not something that will cover all memory devices. We believe that the importance of AS memory, which contains logic inside DRAM, will increase. After all, the direction that Rambus is taking is simple memory (and there are competing devices such as SDRAM and CDRAM even here). Therefore, even if Rambus spreads, there will always be room in the market for AS memory, SDRAM, CDRAM, VRAM, and FBRAM.

12) Even if Rambus gains popularity, that will be at least several years from now. Therefore, even if we sign an agreement now and develop RDRAM, we will not be able to recoup our investment for the foreseeable future.

13) Although it is true that Rambus Inc. has made demo boards and is continuing to actively develop the market, there is also a rumor that the company is in financial trouble. It must be because neither makers nor users are very interested.

14) Because some concerns remain, we cannot reach a clear conclusion. Based on the points raised above, we will continue to watch the trend.

15) Even if Rambus does not become widespread, said patent (if granted) will remain. Therefore, we must thoroughly investigate the DRAM-related claims, if not those related to the bus, and make efforts to avoid [these claims]. We will pay special attention to SDRAM, which is a similar idea. We will also carefully study prior art related to low-skew clock generators.

End of report

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IDEM JOB 03-03-011

MEC 001441

To: LU RAM GR → Arimoto CS
LD RAM GR → Kikuta F
LS RAM GR → Yamagata CS

CC: L Design I B
System Development [Illeg.]

Memo I J

Desired retention period
Receiving side decision
Original retention period

Response deadline

From: L Design I, Patent Committee Member [Seal: Nishimura, LS RAM GR, 3/12/93]
L New RAM Dosaka

Subject; Rambus patent determination request

A need has arisen to evaluate in detail all of the claims in a patent being applied for by Rambus (1 patent, a total number of claims is 150), and therefore, a decision has been made to share the task with System Development and Memo I. L Design I has selected the following claims to evaluate.

Claims 82 through 90: LD RAM Kikuta T
124 through 134: LU RAM Arimoto CS
135 through 150: LS RAM Yamagata CS

Please make your determination by March 17 according to the guideline described below. Please note that agreements have already been obtained from these individuals, and a patent gazette has been distributed to them.

Guideline
① Do not discuss Rambus interface.
② Determine whether or not any other areas contain technologies that will be important in increasing memory speed in the future.
③ A single line of comment, a determination result, and the basis for the determination should be described for each of all claims.
④ Retain notes, etc. that you take when making the determination as well.

Note:
We will hold a small meeting regarding the determination results on 3/18 (Thu.). (Dosaka will contact each individual separately.)
Please adhere to the deadline. (Nishimura)
Thank you.

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IDEM JOB 03-03-011

MEC 001748

To: Shimonishi TB, System Development [Seal: Shimonishi, M Media TB, [Illeg.]]

Evaluation of the DRAM portion of the Rambus DRAM

9/16/93 [Illeg.] [Seal: [Illeg.]]
Ogawa

	(Title)	(Remarks)
Claim 82	Parallel <---> Serial conversion *Known in DRAM nibble mode, etc.	Internal bus is converted into a sequential bit string by multiple sense amplifier string.
Claim 85	2 banks *This is also being done by SDRAM. Need a prior art.	Has multiple active banks inside a chip.
Claim 86	16-way decoding *Up to 24 exist.	One decoder selects [one of the[?]]16 sense amplifiers.
Claim 88	Latches onto a sense amplifier *Known in FIFO, etc., I think.	Sense amplifier has a latch.
Claim 89	Auto precharge I think this is just a simple protocol, and is being implemented in SDRAM, etc.	Automatically precharges
Claim 90	Internal interleaving	Internally interleaves
Claim 91	Pad placement	Uniform intervals
Claim 92	Related to wire length	Wire is 4 mm or shorter, and same for other pins

The above-listed items are relevant. [Seal: Ichihara, D Des. III K, 9/17/93]

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