UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR U.K. LTD., AND HYNIX SEMICONDUCTOR DEUTSCHLAND GMBH, PLAINTIFFS, VS. RAMBUS, INC., DEFENDANT.	C-00-20905 RMW SAN JOSE, CALIFORNIA MARCH 24, 2004 PAGES 1-111

TRANSCRIPT OF PROCEEDINGS
BEFORE THE HONORABLE RONALD M. WHYTE
UNITED STATES DISTRICT JUDGE

A P P E A R A N C E S:

FOR THE PLAINTIFF: TOWNSEND & TOWNSEND & CREW
BY: THEODORE G. BROWN, III AND
JORDAN TREND JONES
379 LYTTON AVENUE
PALO ALTO, CALIFORNIA 94301

THELEN, REID & PRIEST
BY: KENNETH L. NISSLY AND
SUSAN VAN KEULEN
225 WEST SANTA CLARA STREET
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SAN JOSE, CALIFORNIA 95113

ALSO PRESENT: DAVID L. TAYLOR

APPEARANCES CONTINUED ON NEXT PAGE

OFFICIAL COURT REPORTER: LEE-ANNE SHORTRIDGE, CSR, CRR
CERTIFICATE NUMBER 9595

APPEARANCES (CONTINUED)

FOR THE DEFENDANT: MUNGER, TOLLES & OLSON
BY: PETER A. DETRE,
GREGORY P. STONE AND
JENNIFER L. POLSE
33 NEW MONTGOMERY STREET
NINETEENTH FLOOR
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RAMBUS, INC.
PAUL M. ANDERSON, PATENT COUNSEL
4440 EL CAMINO REAL
LOS ALTOS, CALIFORNIA 94022

ALSO PRESENT: ROBERT J. MURPHY

SAN JOSE, CALIFORNIA MARCH 24, 2004

P R O C E E D I N G S

(WHEREUPON, COURT CONVENED AND THE FOLLOWING PROCEEDINGS WERE HELD:)

THE CLERK: CALLING CASE C-00-20905, HYNIX SEMICONDUCTOR VERSUS RAMBUS, ON FOR HEARING ON MOTIONS FOR SUMMARY JUDGMENT.

COUNSEL, STATE YOUR NAME FOR THE RECORD, YOUR HONOR.

MR. BROWN: THEODORE BROWN, YOUR HONOR. FROM TOWNSEND & TOWNSEND & CREW. WITH ME IS MY PARTNER, JORDAN JONES; AND WE HAVE KEN NISSLY AND SUSAN VAN KEULEN FROM THELEN, REID & PRIEST; AND OUR EXPERT, DAVID TAYLOR.

MR. DETRE: GOOD AFTERNOON, YOUR HONOR. PETER DETRE, MUNGER, TOLLES & OLSON FOR RAMBUS, AND WITH ME ARE GREG STONE AND JENNIFER POLSE FROM MUNGER, AND ROBERT MADERO, WHO'S DOING OUR GRAPHICS; PAUL ANDERSON FROM RAMBUS; AND MR. MURPHY, OUR EXPERT, IS IN THE AUDIENCE.

THE COURT: ALL RIGHT. RATHER THAN INDICATE NOW, BECAUSE I MAY HAVE ADDITIONAL MATTERS THAT I WANT TO ASK FOR BRIEFING ON, MAKE SURE SOMEBODY REMINDS ME AT THE END THAT THERE ARE A COUPLE OF THINGS THAT I WANT SOME FURTHER

INFORMATION ON.

BUT WITH THAT, HAVE YOU DONE WHAT YOU DID YESTERDAY AND WORK OUT BETWEEN YOURSELVES THE ORDER THAT YOU WANT TO PROCEED ON, OR --

MR. BROWN: ACTUALLY, WE DID NOT.

THE COURT: OKAY.

MR. BROWN: IS THERE AN ORDER THAT YOU WOULD, THAT YOU WOULD LIKE TO HEAR THE ISSUES ON?

THE COURT: WELL, WHY DON'T WE GO THROUGH AND SEE IF WE CAN'T FIGURE OUT WHAT MIGHT BE A -- I THINK I'M PARTICULARLY INTERESTED IN THE MOTION DEALING WITH THE BLOCK SIZE INFORMATION, THE OPERATIONS CODE, AND THE SECOND EXTERNAL CLOCK SIGNAL.

SO WHY DON'T WE DO THOSE THREE FIRST, AND THEN WE'LL COVER THE OTHERS.

MR. BROWN: OKAY.

MR. DETRE: YOUR HONOR, I THINK YOU MEAN HYNIX'S MOTIONS, BECAUSE RAMBUS ALSO HAS A MOTION FOR SUMMARY JUDGMENT WHICH DISCUSSES AT LEAST A COUPLE OF THOSE.

THE COURT: RIGHT. I WAS NOT TRYING TO LIMIT IT TO EITHER YOUR MOTION OR THEIR MOTION.

MR. DETRE: OH, I SEE.

THE COURT: THOSE ARE THE ISSUES, THE

ONES THAT INVOLVE ISSUES PERTAINING TO THOSE ITEMS.

MR. DETRE: OKAY. DO YOU HAVE A PREFERENCE AS TO WHETHER WE DO RAMBUS'S MOTION FIRST OR HYNIX'S MOTIONS?

THE COURT: SHOULDN'T WE DO THEM AT THE SAME TIME TO THE EXTENT THAT THEY OVERLAP?

MR. BROWN: I'LL ADDRESS BLOCK SIZE, YOUR HONOR.

THE COURT: OKAY. IS THAT OKAY THAT HE GOES FIRST ON BLOCK SIZE?

MR. DETRE: THAT WOULD BE FINE, YOUR HONOR. I THINK ACTUALLY, IN THAT CASE, VERY SIMILAR ISSUES ARE RAISED BY --

MR. BROWN: BOTH MOTIONS.

MR. DETRE: -- BOTH MOTIONS.

THE COURT: OKAY.

MR. BROWN: IT'LL TAKE ME JUST A MINUTE, YOUR HONOR.

THE COURT: OKAY.

MR. BROWN: OKAY, BLOCK SIZE INFORMATION.

AND BECAUSE I HAVE NOT COMPLETELY REVAMPED THIS FROM WHAT I HAD IN MIND YESTERDAY, OR IN VIEW OF YESTERDAY'S DISCUSSION, WHAT I'M GOING TO DO, I'VE PRESENTED THE TWO CLAIM CONSTRUCTIONS HERE, BUT FROM THE TENTATIVE RULING, BASICALLY IT

APPEARS, AT LEAST TENTATIVELY, THAT THE COURT'S INCLINED TO ADOPT SOMETHING THAT'S PRETTY SIMILAR TO HYNIX'S CONSTRUCTION, SO I'M MOSTLY GOING TO TALK ABOUT THAT.

THERE ARE TWO REASONS WHY HYNIX, WHY THE ACCUSED PRODUCTS DO NOT USE BLOCK SIZE INFORMATION UNDER THIS CONSTRUCTION.

ONE OF THOSE REASONS ALSO APPLIES TO THE PROPOSED RAMBUS CONSTRUCTION.

FIRST, THE BLOCK SIZE INFORMATION, OR WHAT -- MORE PROPERLY WHAT RAMBUS SAYS REPRESENTS BLOCK SIZE INFORMATION IN THE ACCUSED PRODUCTS DOES NOT TRANSFER, DOES NOT SPECIFY OR REPRESENT THE TOTAL AMOUNT OF DATA THAT IS TO BE TRANSFERRED ON THE BUS, AND IT DOESN'T EVEN SPECIFY A QUANTITY OF DATA WHICH IS TO BE TRANSFERRED ON THE BUS OR TRANSFERRED DURING A MEMORY OPERATION.

AND I'M GOING TO GO BACK HERE, THIS IS A LITTLE BIT ON CLAIM CONSTRUCTION ISSUES, AND THE COURT WILL RECALL THAT BLOCK SIZE INFORMATION, WHICH IS DISCLOSED IN THE PATENT, IS A FIELD WITHIN THE REQUEST PACKET THAT SPECIFIES THE AMOUNT OF DATA, OR THE SIZE OF THE BLOCK TO BE TRANSFERRED IN RESPONSE TO THE REQUEST.

AND WHAT I WANT TO DO IS I'LL GO BACK TO

THE -- WE'VE SEEN THIS SLIDE BEFORE -- THIS IS A FAIRLY TYPICAL SDRAM SYSTEM TOPOLOGY THAT WE TALKED ABOUT LAST THURSDAY IN THE TUTORIAL, AND TYPICALLY THE INDIVIDUAL -- THIS IS SDRAMS, THIS IS CLOSELY ANALOGOUS TO A DDR SDRAM SYSTEM, THAT TYPICALLY THESE CHIPS ARE MOUNTED ON INDIVIDUAL CIRCUIT CARDS THAT, TOGETHER, FORM MODULES.

AND, FOR EXAMPLE, THERE WILL BE PERHAPS TWO CHIPS OR FOUR CHIPS OR EIGHT CHIPS OUTPUTTING DATA IN PARALLEL TO SEPARATE SECTIONS OF THE DATA BUS.

SO, FOR EXAMPLE, IF WE HAD FOUR CHIPS ON A MODULE THAT WERE CONFIGURED IN A BY EIGHT CONFIGURATION, THAT IS, WITH EIGHT DATA I/O LINES FOR EACH CHIP, THAT THOSE CHIPS WOULD BE OPERATED SUBSTANTIALLY SIMULTANEOUSLY TO OUTPUT A 32-BIT WORD, OR 32 BITS IN PARALLEL AT A TIME.

THE BURST LENGTH, WHICH, AS WE'VE ALREADY DISCUSSED, CAN BE PROGRAMMED IN THE MODE REGISTER, SPECIFIES THE -- IN THE ABSENCE OF ANY OTHER COMMANDS, IT BASICALLY SAYS HOW MANY BITS WILL COME OUT SERIALLY ON EACH PIN.

AND THE TOTAL AMOUNT OF DATA, WHICH IS RETRIEVED FROM EACH DEVICE, OR EACH SDRAM CHIP HERE, DEPENDS NOT ONLY ON THE NUMBER OF BITS THAT

WOULD BE OUTPUT SERIALLY ON EACH PIN, BUT IT ALSO DEPENDS ON THE NUMBER OF DATA I/O PINS ON THE BUS.

SO THE BURST SIZE, OR THE BURST LENGTH, DOES NOT SPECIFY THE TOTAL AMOUNT OF DATA, OR DOES NOT EVEN REPRESENT THE TOTAL AMOUNT OF DATA WHICH IS TO BE OUTPUT IN RESPONSE TO A READ COMMAND.

THE SECOND THING IS THAT -- OR THE SECOND POINT ON THIS ISSUE THAT I WANT TO RAISE IS THAT THE MEMORY CONTROLLER, WHEN IT IS ASKING FOR DATA, IS BASICALLY -- BASICALLY IT WILL BE ASKING FOR TWO OR FOUR OR FIVE OR EIGHT SORT OF 32-BIT WORDS, IN THIS CASE OF DATA FROM A MEMORY MODULE, AND THE MEMORY CONTROLLER DOES NOT CARE HOW MANY BITS ARE RETRIEVED FROM EACH PIN, OR SORRY, IT DOES CARE HOW MANY BITS ARE RETRIEVED FROM EACH PIN.

BUT IT DOESN'T CARE HOW MANY MEMORY CHIPS ARE RETRIEVED FROM EACH MEMORY CHIP ON THE MODULE.

THAT IS, IF A MEMORY CONTROLLER SENDS AN ACTIVATE COMMAND AND THEN A READ COMMAND TO, SAY, BANK 0, OR THE FIRST MEMORY MODULE THERE, WHAT IT CARES ABOUT -- AND I'LL ASSUME HERE THAT IT'S NOT SENDING ANY OTHER COMMANDS -- IS THAT IT WANTS TO GET FOUR, FOR A BURST LENGTH OF FOUR, IT WANTS TO GET FOUR 32-BIT CHUNKS OF DATA IN PARALLEL OFF THAT MODULE.

AND THE CONTROLLER DOESN'T CARE WHETHER THERE ARE TWO CHIPS, EACH OF WHICH HAS 16 DATA I/O LINES ON THAT MODULE, OR WHETHER THERE ARE FOUR CHIPS, EACH OF WHICH HAS EIGHT DATA LINES ON A CHIP, OR WHETHER IT HAS EIGHT CHIPS ON THAT MODULE, EACH OF WHICH HAS FOUR DATA LINES.

IN EACH CASE, IN EACH CASE IT'S GETTING CHUNKS OF 32-BIT WORDS IN PARALLEL.

SO THAT THE MEMORY CONTROLLER DOESN'T CARE HOW MUCH DATA, AND IN GENERAL DOESN'T KNOW HOW MUCH DATA, IT'S GETTING FROM ANY INDIVIDUAL CHIP. ALL IT KNOWS, OR ALL IT WOULD KNOW IN THAT CIRCUMSTANCE IS HOW MUCH DATA IT'S GETTING FROM THE MODULE AS A WHOLE.

AND MR. MURPHY IN HIS DEPOSITION AGREED WITH US, AND BASICALLY MR. MURPHY SAID, AFTER BASICALLY I'D GONE THROUGH THIS KIND OF AN EXPLANATION, WAS THAT THE CONTROLLER KNOWS HOW MANY BITS TO OUTPUT, HOW MANY BITS SHOULD BE OUTPUT PER MODULE, AND HE AGREED WITH THAT.

AND THE CONTROLLER DOES NOT NECESSARILY KNOW OR CARE HOW MANY BITS ARE OUTPUT PER CHIP, AND MR. MURPHY AGREED THAT THE CONTROLLER, THAT HE DIDN'T THINK THE CONTROLLER CARED HOW MANY BITS WERE OUTPUT PER CHIP.

SO THE BURST LENGTH THAT RAMBUS SAYS IS EQUIVALENT TO BLOCK SIZE INFORMATION, IT DOES -- IS NOT BLOCK SIZE INFORMATION BECAUSE IT DOES NOT SPECIFY THE TOTAL AMOUNT OF DATA THAT IS TO BE OUTPUT FROM A CHIP.

SECOND, AND THIS IS ALSO A SLIDE THAT YOUR HONOR HAS SEEN BEFORE, LAST THURSDAY, BUT JUST TO REVIEW BRIEFLY, THAT IN ORDER TO RETRIEVE DATA FROM A CHIP, FIRST WHAT YOU HAVE TO DO IS YOU HAVE TO SEND AN ACTIVATE COMMAND TO THE CHIP TO OPEN A ROW, AND THEN, AT LEAST IN EITHER SDRAM OR DDR, AFTER THAT YOU SEND A READ COMMAND WITH THE COLUMN ADDRESS.

AND IN THE ABSENCE OF ANY FURTHER COMMANDS, THE RESULT WILL BE THAT ON EACH PIN -- SORRY -- ON EACH PIN, THERE WILL BE FOUR DATA BITS OUTPUT SERIALLY FOR A BURST LENGTH OF FOUR.

AND I'VE BEEN CAREFUL TO SAY IN THE TUTORIAL AND HERE THAT IN THE ABSENCE OF ANY FURTHER COMMANDS, BECAUSE THE CONTROLLER CAN ISSUE OTHER COMMANDS THAT CHANGE THE TOTAL AMOUNT OF DATA THAT COMES OUT PER PIN AND, OF COURSE, CAN CHANGE THE TOTAL AMOUNT OF DATA WHICH COMES OUT PER CHIP.

THE CONTROLLER IS NOT STUCK WITH GETTING BITS OUT FOUR BITS AT A TIME ON A PIN.

OKAY. THERE ARE A NUMBER OF OTHER SEQUENCES OF COMMANDS OR OPERATIONS THAT THE CONTROLLER CAN DO IF IT WANTS, THAT IT IS CAPABLE OF DOING THAT CHANGE THE NUMBER OF BITS THAT ARE OUTPUT ON EACH PIN.

THIS IS JUST ANOTHER EXAMPLE, A SOMEWHAT SIMPLIFIED PICTURE, AND THIS IS FROM TAYLOR EXHIBIT 66 WITH AN SDRAM, AND IT BASICALLY SHOWS THE SAME INFORMATION THAT WAS ON THE PREVIOUS PAGE, EXCEPT IT SHOWS IT IN A SOMEWHAT SIMPLIFIED FORM.

THERE IS AN ACTIVATE COMMAND, THEN THERE IS A READ COMMAND, AND THEN AFTER, OR AT APPROXIMATELY -- ON THE THIRD CLOCK CYCLE, BECAUSE THIS IS A CAS LATENCY SYSTEM, YOU START GETTING THE BITS OUT AND YOU ARE GET FOUR BITS IN BURST LENGTH FOUR, FOUR BITS OUT SERIALLY PER PIN.

NOW, ON THE OTHER HAND, IF THE CONTROLLER -- AND BASICALLY THIS IS NOW A CAS LATENCY 2 SYSTEM.

BUT IF THE CONTROLLER DOES AN ACTIVATE COMMAND AND THEN DOES A READ COMMAND WITH THE COLUMN ADDRESS, TWO CYCLES LATER THE BITS WILL START COMING OUT FROM THAT READ COMMAND.

NOW, BUT IF THE CONTROLLER ON, IN THIS CASE, THE NEXT CLOCK CYCLE ISSUES A SECOND READ

COMMAND WITH A, WITH A SECOND COLUMN ADDRESS, THE THREE BITS THAT WOULD HAVE COME OUT IN RESPONSE TO THE FIRST READ COMMAND DO NOT COME OUT ANYMORE.

OKAY. TWO CYCLES AFTER THE SECOND READ COMMAND, THE BITS STARTING AT THE COLUMN ADDRESS SPECIFIED WITH THE SECOND READ COMMAND ARE OUTPUT ON EACH PIN.

SO IF THE CONTROLLER WANTS, FOR EXAMPLE, FIVE BITS OUTPUT PER PIN, THEN IT CAN STACK -- IT CAN BASICALLY PUT TWO READ COMMANDS TOGETHER IN THIS WAY AND IT WILL GET FIVE BITS.

IF, FOR EXAMPLE, INSTEAD OF HAVING THE SECOND READ COMMAND ONE CLOCK CYCLE AFTER THE FIRST CLOCK CYCLE, IF WE HAD HAD THE SECOND READ COMMAND TWO BITS, OR TWO CYCLES AFTER THE FIRST READ CYCLE, OR THE FIRST READ COMMAND, THEN WE WOULD GET TWO BITS OUTPUT ON EACH PIN IN RESPONSE TO THE FIRST READ COMMAND, AND THE SECOND READ COMMAND WOULD TERMINATE THAT FIRST READ AFTER TWO BITS.

AND IN THE ABSENCE OF ANY FURTHER COMMANDS, IT WOULD THEN -- THERE WOULD BE FOUR BITS OUTPUT IN RESPONSE TO THE SECOND READ COMMAND, AND IN THIS, THIS SITUATION WHERE THERE ARE TWO CLOCK CYCLES SEPARATED BETWEEN READ COMMANDS, YOU WOULD GET A TOTAL OF SIX BITS OUT PER PIN.

THE COURT: SO WHAT?

MR. BROWN: HUM?

THE COURT: SO WHAT? WHY DOES THIS MAKE A DIFFERENCE?

MR. BROWN: WELL, WHAT I'M SAYING IS THAT THE -- WELL, WHY IT MAKES A DIFFERENCE IS THAT THE BURST LENGTH, OKAY, IN RESPONSE TO THE FIRST READ COMMAND, OKAY, THE BURST LENGTH IS IRRELEVANT TO HOW MANY BITS COME OUT.

IT MAY SET A MAXIMUM NUMBER OF BITS THAT CAN COME OUT IN RESPONSE TO THAT FIRST READ COMMAND, OKAY, BUT DEPENDING ON WHAT THE CONTROLLER DOES AFTER THAT AND DEPENDING ON HOW MANY BITS THE CONTROLLER WANTS, OKAY, THE NUMBER OF BITS WHICH ARE OUTPUT IN RESPONSE TO THE FIRST COMMAND IS NOT EQUAL TO THE, TO THE BURST LENGTH.

AND UNDER THE, THE TENTATIVE RULING, THE TENTATIVE CONSTRUCTION THAT, THAT THE COURT HAS, THE BURST LENGTH DOES NOT SPECIFY OR INDICATE THE NUMBER OF BITS TO BE TRANSFERRED ON THE BUS IN RESPONSE TO -- IN A READ OPERATION.

OKAY. THE NUMBER OF BITS THAT CAN BE TRANSFERRED ON THE BUS IN THIS WHOLE READ OPERATION WITH TWO READ COMMANDS IS FIVE, WHICH HAS NOTHING TO -- THERE'S NO NECESSARY RELATIONSHIP TO THE

BURST LENGTH.

IF YOU TAKE THE FIRST READ COMMAND AS THE FIRST READ OPERATION, THEN YOU ONLY GET, IN THIS SITUATION, ONE BIT OUT IN RESPONSE TO THAT READ, TO THAT FIRST READ COMMAND, EVEN THOUGH THE BURST LENGTH IS SET TO FOUR.

THIS IS A SOMEWHAT FURTHER -- THIS IS A FURTHER EXAMPLE WHERE NOW THE CONTROLLER WANTS TEN BITS OUT PER PIN, AND THIS IS PRESSING MY POWER POINT SKILLS, BUT BASICALLY WE HAVE THREE READ COMMANDS. THE FIRST TWO READ COMMANDS ARE SPACED BY FOUR CLOCK CYCLES, AND THAT MEANS THAT IN RESPONSE TO THE FIRST READ COMMAND, YOU DO GET FOUR BITS OUT SERIALLY PER PIN.

IN RESPONSE TO THE -- AND THEN -- BUT THEN THERE'S A THIRD READ COMMAND, WHICH IS TWO CLOCK CYCLES AFTER THE SECOND.

AS A RESULT, THE THIRD READ COMMAND INTERRUPTS THE SECOND READ COMMAND AND ONLY TWO BITS ARE OUTPUT IN RESPONSE TO THE, TO THE SECOND READ COMMAND, BUT FOUR ARE OUTPUT IN RESPONSE TO THE THIRD READ COMMAND.

AGAIN, IN THE MIDDLE HERE, WE HAVE A READ OPERATION WHERE THE NUMBER OF BITS OUTPUT ON A PIN IS NOT EQUAL TO THE PREPROGRAMMED BURST LENGTH OF

FOUR IN THIS EXAMPLE.

NOW, THERE'S ANOTHER CONTROL SIGNAL WHICH I HAVE NOT YET EXPLICITLY, OR THAT WE HAVEN'T DISCUSSED, AND IT'S A CONTROL SIGNAL WHICH IS PRESENT ON BOTH READ AND WRITE OPERATIONS IN AN SDRAM, AND THAT'S WHAT'S KNOWN AS A DATA MASS.

OKAY. IN ADDITION IN RAS, CAS, WRITE ENABLE AND CHIP SELECT, AND THERE ARE -- IT IS SHOWN DOWN HERE AS A DQM SIGNAL, AND THAT IS A SIGNAL WHICH, UNDER -- THAT THE CONTROLLER CAN ISSUE TO MASK A PARTICULAR BIT OR SET OF BITS.

THERE ARE ACTUALLY TWO MASK OPERATIONS SHOWN HERE, ONE FOR A WRITE OPERATION AND ONE FOR A READ OPERATION, AND I'LL DISCUSS THE ONE PARTICULARLY FOR A READ OPERATION.

OVER AT THE LEFT-HAND SIDE OF THIS TIMING DIAGRAM, WE'VE OPENED A ROW.

THEN THERE IS A READ COMMAND AND NOTHING ELSE HAPPENS, SO WE GET FOUR BITS OUTPUT ON THE DATA LINE.

THEN THERE IS A WRITE COMMAND, WHICH I'LL IGNORE FOR JUST A MOMENT.

AND THEN FOLLOWING THAT WRITE COMMAND, THERE IS YET ANOTHER READ COMMAND.

NOW -- THIS IS ALL, AGAIN, WITH A BURST

LENGTH SET AT FOUR.

TWO CYCLES AFTER THAT SECOND READ COMMAND, THE COMMAND THAT'S CLOSEST TO THE RIGHT, THE CONTROLLER IN THIS CASE, CAN ASSERT THE DQM, OR THE DATA MASK SIGNAL.

NOW, WHAT THAT MEANS IN THAT CASE, AND THE SIGNAL RISING RIGHT HERE IS WHERE IT IS SHOWING THAT THE DATA MASK IS BEING ASSERTED -- TWO CYCLES AFTER THE ASSERTION OF THAT DATA MASK, THE EFFECT IS THAT IT SUPPRESSES THAT THIRD BIT OUTPUT IN THAT SERIES OF FOUR.

SO, AGAIN, THE NUMBER OF BITS WHICH ARE TRANSFERRED PER PIN IN THIS CASE IS NOT EQUAL TO THE BURST LENGTH.

THAT IS, THE CONTROLLER, BY ASSERTING THIS DATA MASK SIGNAL, CAN EFFECTIVELY PREVENT THE OUTPUT OF THE THIRD BIT IN THAT SERIES.

THE COURT: THE FACT THAT IT COULD DO IT DOESN'T MEAN THAT IT NECESSARILY DOESN'T INFRINGE, DOES IT, OR MEET THE LIMITATION IF IT COULD MEET THE LIMITATION?

MR. BROWN: IF IT COULD MEET THE LIMITATION, THEN PERHAPS IT COULD INFRINGE.

WHAT I'M TRYING TO SHOW HERE IS THE BURST LENGTH, WHICH IS PROGRAMMED INTO THE -- THAT IS

PROGRAMMED INTO THE REGISTER HAS NO NECESSARY RELATIONSHIP TO THE NUMBER OF BITS WHICH ARE OUTPUT.

EACH -- THE CONTROLLER BASICALLY, IT'S A RARE -- IT WOULD BE A RARE SITUATION WHERE THE CONTROLLER ALWAYS WANTS EXACTLY THE SAME NUMBER OF BITS.

IT -- THERE ARE TIMES WHEN IT WANTS TWO BITS, THERE ARE TIMES WHEN IT WANTS ONE BIT, THERE ARE TIMES WHEN IT WANTS THREE BITS OR FOUR BITS OR SOME OTHER NUMBER OF BITS, AND IT MAY NOT WANT THE BITS FROM SEQUENTIAL COLUMN ADDRESSES, WHICH ARE WHAT IS GENERATED INTERNALLY.

SO IT MAY -- THE CONTROLLER MAY WANT JUST THE FIRST, SECOND AND FOURTH BITS, OKAY, AND NOT WANT THE THIRD BIT.

SO WHAT IT DOES IN THIS CASE IS IT ASSERTS THE DATA MASK SO THAT IT DOES NOT -- IT CHOOSES NOT TO GET THE THIRD BIT.

OKAY. THE BURST LENGTH, WHICH IS SET IN THE MODE REGISTER, IS JUST SET AS SORT OF A DEFAULT OF THE NUMBER OF INTERNAL COLUMN ADDRESSES WHICH ARE GENERATED IN THE CHIP AND HAS NOTHING, HAS NO NECESSARY RELATION AND NO PARTICULAR RELATION TO THE NUMBER OF BITS WHICH ARE ACTUALLY OUTPUT IN

RESPONSE TO A READ COMMAND OR IN RESPONSE TO A SERIES OF READ COMMANDS.

THERE IS A SIMILAR DATA MASKING OPERATION ON THE WRITE, ON THE WRITE OPERATION, WHICH WE HAVE NOT TALKED ABOUT A WHOLE LOT, EXCEPT THAT WHEN THERE IS A DATA MASK SIGNAL ASSERTED ON THE WRITE OPERATION, WHICH IS WHAT IS SHOWN HERE, BASICALLY IT PREVENTS THIS, THE THIRD BIT IN THAT SEQUENCE, AT THE SAME TIME AS THE DATA MASK, FROM BEING TRANSFERRED TO THE MEMORY CHIP.

THERE'S A SIMILAR KIND OF OPERATION, AND I'M GOING TO TRY AND GO THROUGH THIS RELATIVELY QUICKLY, IN DDR.

IN THE DDR SDRAM FOLLOWING AN ACTIVATE COMMAND, AND THEN FOLLOWING -- AND THEN WITH A READ COMMAND, THEN TWO CYCLES LATER IN A CAS LATENCY SYSTEM, THERE WILL BE FOUR BITS OUTPUT IN THE ABSENCE OF ANY FURTHER COMMANDS.

AND THIS IS JUST AN EXAMPLE OF BASICALLY TWO BACK-TO-BACK COMMANDS, TWO BACK-TO-BACK READ COMMANDS WHERE, WHICH ARE SPACED BY TWO CLOCK CYCLES. TWO CLOCK CYCLES IS SUFFICIENT TO, IN THE NORMAL SCHEME OF THINGS, TO OUTPUT FOUR BITS OF DATA.

SO IN THIS READ OPERATION, THERE ARE TWO

READ COMMANDS, AND AS A RESULT, THERE ARE A TOTAL OF EIGHT BITS OF DATA THAT ARE OUTPUT.

HOWEVER, IF THE SECOND READ COMMAND IS ISSUED ONE CLOCK CYCLE AFTER THE FIRST READ COMMAND, THEN THE SECOND READ COMMAND WILL TERMINATE THE FIRST BURST READ AND ONLY TWO BITS WILL BE OUTPUT IN RESPONSE TO THE FIRST READ COMMAND, EVEN THOUGH THE BURST LENGTH IS SET TO FOUR.

SO THE BURST LENGTH IS A CONVENIENCE, BUT IT DOES NOT GOVERN HOW MANY BITS ARE OUTPUT IN RESPONSE TO A READ COMMAND.

THERE ARE ALSO OTHER WAYS OF INTERRUPTING THE BURST, AGAIN, UNDER THE CONTROL OF THE CONTROLLER.

THIS IS A COMMAND THAT WE HAVE NOT SEEN BEFORE, BUT IT IS AN ALTERNATE COMMAND WHICH CAN BE USED IN EITHER THE SDRAM OR THE DDR SDRAM, AND THAT IS PRECHARGE COMMAND.

AND THIS IS AN EXAMPLE OF WHERE -- AND WE TALKED ABOUT PRECHARGING AND WHAT PRECHARGING DOES. AS YOUR HONOR WILL RECALL, IT BASICALLY TAKES THE DATA WHICH IS ON THE SENSE AMPLIFIERS AND READS IT BACK INTO THE CELLS AND PREPARES THE BIT LINES AND THE SENSE AMPLIFIERS FOR THE NEXT READ OPERATION OR

THE NEXT WRITE OPERATION.

AND IN THIS CASE, THERE IS A PRECHARGE COMMAND GIVEN ONE CYCLE AFTER THE READ COMMAND AND, AS A RESULT, THE BURST IS INTERRUPTED AFTER TWO BITS EVEN THOUGH THE, THE BURST LENGTH IS SET TO FOUR IN THAT CASE.

THERE'S ALSO A BURST STOP COMMAND IN BOTH SDRAM AND DDR THAT -- IF THE CONTROLLER ISSUES IT, IF IT ONLY WANTS TWO BITS, THEN WHAT IT DOES IS IT CAN ISSUE A BURST STOP COMMAND AND THE BURST TERMINATES. YOU ONLY GET TWO BITS OUT, OUTPUT FROM THE CHIP IN RESPONSE TO THE READ COMMAND EVEN THOUGH, AGAIN, THE BURST LENGTH IS SET TO FOUR.

THE COURT: HOW WOULD YOU DEFINE "BURST" OR "BURST LENGTH"?

MR. BROWN: HOW WOULD I DEFINE THE BURST?

THE COURT: IF I WERE TO ASK YOU, "WHAT DOES THAT TERM MEAN" --

MR. BROWN: THE BURST LENGTH IS THE -- SORRY. REMEMBER, BACK ON THURSDAY, THERE WAS A MODE REGISTER ON THE SDRAM AND ON THE DDR.

THE COURT: RIGHT.

MR. BROWN: AND THERE WAS A CODE IN THERE. THERE ARE THREE, THREE BITS IN THE MODE REGISTER THAT SPECIFY WHAT THE BURST LENGTH IS,

OKAY, THAT WILL SET IT TO EITHER TWO OR FOUR OR EIGHT.

OKAY. AND THAT IS THE, THE TWO OR FOUR OR EIGHT IS THE NUMBER OF BITS THAT, IN THE ABSENCE OF ANYTHING ELSE, ANY OTHER ACTION TAKEN BY THE CONTROLLER, THAT IS THE NUMBER OF BITS THAT WILL COME OUT IN RESPONSE TO A READ COMMAND.

AND THAT IS -- IT'S THAT BURST LENGTH WHICH IS PROGRAMMED INTO THE CONTROLLER THAT IS ACCUSED OF, THAT RAMBUS ACCUSES OF BEING THE SAME AS BLOCK SIZE INFORMATION IN THEIR CLAIMS.

AND THAT IS THE SOLE FEATURE OF THE, THE SOLE FEATURE IN THE ACCUSED PRODUCTS THAT RAMBUS HAS IDENTIFIED AS BEING EQUIVALENT TO OR THE SAME AS THE BLOCK SIZE INFORMATION IN THEIR CLAIMS.

THE COURT: OKAY.

MR. BROWN: AND BASICALLY MR. MURPHY AGREED IN HIS DEPOSITION, AND I'VE GOT THE PAGES CITED HERE, WE DID FILE THIS YESTERDAY AND I HAVE EXTRA COPIES OF THE DEPOSITION DESIGNATIONS FOR YOU, YOUR HONOR.

AND IN PARTICULAR ON THIS ISSUE, I THINK THAT THESE ARE THE, THE RELEVANT PAGES ARE 136, LINE 18 TO 142, LINE 10; AND 143 LINE 89 TO 145, LINE 17.

BUT IN PARTICULAR, ON PART OF THIS AT PAGE 141, MR. MURPHY AGREED THAT THE CONTROLLER IS WHAT CONTROLS THE NUMBER OF BITS WHICH ARE OUTPUT IN RESPONSE TO A READ COMMAND. IT'S NOT THE BURST LENGTH.

THE CONTROLLER IS NOT TIED TO GETTING BITS FROM THE MEMORY IN CHUNKS EQUAL TO THE BURST LENGTH. BASICALLY THE CONTROLLER MAKES THE DECISIONS, AND IF THE CONTROLLER WANTS FIVE BITS, IT CAN DO THAT. IF IT WANTS THREE BITS, IT CAN DO THAT.

AND EVENTUALLY, THERE WERE -- THE RECORD IS NOT AS CLEAN AS I WOULD LIKE, BUT THE CONTROLLER CAN PICK ANY NUMBER OF BITS TO COME OUT PER PIN, REGARDLESS OF WHETHER THE BURST LENGTH IS SET TO TWO OR FOUR OR EIGHT.

AND MR. MURPHY AGREED THAT THE NUMBER OF BITS OF INFORMATION COMING FROM THE DEVICE IS A CONTINUOUS -- HE SAYS A CONTINUOUS STREAM OF INFORMATION OF WHATEVER NUMBER OF BITS THAT THE CONTROLLER WISHES TO GET.

AND ACTUALLY, HE ALSO AGREED THAT IT IS NOT NECESSARILY A CONTINUOUS, A CONTINUOUS STREAM BECAUSE OF THE USE OF THE DATA MASKING OPERATION, THAT THE CONTROLLER, IF IT CHOOSES, CAN ISSUE A

DATA MASK WHICH INTERRUPTS THAT STREAM OR CAUSES THE, THE STREAM OF DATA TO BE DISCONTINUOUS.

SO FOR THOSE REASONS -- BASICALLY THE BLOCK SIZE, OR WHAT RAMBUS IDENTIFIES AS BLOCK SIZE INFORMATION DOES NOT SPECIFY THE TOTAL AMOUNT OF DATA THAT IS TO BE TRANSFERRED ON THE BUS DURING A MEMORY READ OR WRITE OPERATION FOR AT LEAST TWO REASONS.

ONE, THE BURST LENGTH THAT IS SET IN THE MODE REGISTER DOES NOT SPECIFY THE TOTAL AMOUNT OF DATA WHICH IS OUTPUT PER CHIP BECAUSE OF THE NUMBER OF -- THE AMOUNT OF DATA WHICH IS OUTPUT PER CHIP DEPENDS ON THE NUMBER OF DATA I/O LINES ON THAT PARTICULAR CHIP IN ADDITION TO THE BURST LENGTH, OR AT LEAST, THAT'S THE MAXIMUM THAT THE, THAT THE CHIP CAN OUTPUT IN RESPONSE TO ONE READ COMMAND.

IN ADDITION, THOUGH, THE BURST LENGTH THAT IS SET IN THE MODE REGISTER HAS NO NECESSARY RELATIONSHIP TO THE NUMBER OF BITS THAT ARE OUTPUT IN RESPONSE TO, DURING A READ OPERATION. THAT'S ENTIRELY UNDER THE CONTROL OF THE CONTROLLER AND THE IDENTIFIER IN THE SEQUENCE IN THE COMMAND THAT IT ISSUES TO THE MEMORY CHIPS.

THE COURT: OKAY. THANK YOU.

MR. BROWN: OKAY.

MR. DETRE: WELL, YOUR HONOR, I'D LIKE TO TAKE MR. BROWN'S TWO POINTS IN ORDER.

FIRST WITH RESPECT TO MR. BROWN'S POINT ABOUT THE TOTAL AMOUNT OF DATA, MR. BROWN SAID THAT THE BURST LENGTH IN THE ACCUSED DEVICES DON'T REPRESENT A TOTAL AMOUNT OF DATA BECAUSE IT DEPENDS ON THE NUMBER OF DATA I/O LINES OR OUTPUT PINS, DATA PINS ON THE DEVICE.

WELL, AS WE'VE DISCUSSED TO SOME EXTENT IN OUR BRIEFING, ANY REASONABLE IDEA OF BEING REPRESENTATIVE, REPRESENTATIVE OF THE TOTAL AMOUNT OF DATA OR SPECIFYING A TOTAL AMOUNT OF DATA WOULD BE SATISFIED BECAUSE A MEMORY DEVICE HAS A FIXED NUMBER OF DATA I/O LINES.

AND SO, FOR EXAMPLE, IF IT'S A BY EIGHT PART, THAT MEANS IT HAS EIGHT DATA PINS, AND IF THE BURST LENGTH IS SET TO FOUR, THEN IN THE NORMAL COURSE -- AND I'LL GET TO MR. BROWN'S SECOND ARGUMENT IN A BIT -- BUT IN THE NORMAL COURSE, UNLESS INTERRUPTED BY ANOTHER COMMAND, IT WILL OUTPUT 32 BITS, FOUR BITS PER PIN, FOUR BITS FOR EACH OF THE EIGHT PINS.

NOW, MR. BROWN WENT ON TO TALK ABOUT MODULES AND HOW, WHEN A CONTROLLER SENDS A READ REQUEST TO A MODULE, IT'LL EXPECT TO GET DATA BACK

FROM EACH OF THE MEMORY CHIPS IN THAT MODULE.

I DON'T THINK THAT MR. BROWN EXPLAINED HOW THIS IS IN ANY WAY RELEVANT TO THE CLAIMS THAT ARE AT ISSUE HERE.

IF WE COULD PULL UP, JUST FOR AN EXAMPLE, ONE OF THE CLAIMS THAT INVOLVE BLOCK SIZE INFORMATION.

HAVE YOU GOT THE '918 PATENT? AND IF WE COULD GO TO CLAIM 18. I'M SORRY. I DON'T HAVE THE PAGE NUMBER HERE, BUT IT'S -- IT'S PAGE 30, AND IT'S ON THE RIGHT-HAND COLUMN, CLAIM 18. THERE WE GO.

THIS REFERS TO A METHOD OF OPERATION OF A SYNCHRONOUS MEMORY DEVICE.

CLAIM 18 OF THE '918 PATENT, AND ALL OF THE OTHER CLAIMS THAT INVOLVE BLOCK SIZE INFORMATION, ARE ON A DEVICE BY DEVICE BASIS. WE'RE TALKING ABOUT THE INDIVIDUAL MEMORY CHIPS, NOT THE MODULES.

AND WHEN A CONTROLLER SENDS A READ REQUEST AND IT GOES TO THE MODULE, THAT READ REQUEST THEN GETS TRANSLATED INTO A READ REQUEST THAT GOES TO EACH OF THE INDIVIDUAL MEMORY CHIPS ON THAT MODULE AND EACH OF THOSE INDIVIDUAL MEMORY CHIPS WILL THEN RESPOND BY OUTPUTTING, FOR EACH

DATA PIN, THE NUMBER OF BITS SPECIFIED BY THE BURST LENGTH.

MR. BROWN ALSO MADE THE POINT THAT THE MEMORY CONTROLLER DOESN'T KNOW OR CARE HOW MANY -- HOW MUCH DATA WILL BE COMING BACK FROM EACH INDIVIDUAL DEVICE.

WELL, AGAIN, IT'S NOT CLEAR TO ME, AGAIN, HOW THAT'S RELEVANT BECAUSE THE BLOCK SIZE INFORMATION IN RAMBUS'S CLAIMS RELATES TO EACH SPECIFIC DEVICE AND NOT TO THE DESIRES OR KNOWLEDGE OF THE MEMORY CONTROLLER.

BUT, IN FACT, IT'S NOT EVEN TRUE THAT THE MEMORY CONTROLLER DOESN'T KNOW HOW MUCH DATA WILL BE COMING BACK FROM EACH MEMORY DEVICE. IT DOES KNOW.

THIS ARGUMENT WAS NOT ACTUALLY MADE IN HYNIX'S BRIEFING, SO WE COULD NOT RESPOND IN OUR BRIEFING, BUT WE DO HAVE A DATA SHEET OF A HYNIX MODULE THAT I DOWNLOADED THE OTHER DAY FROM HYNIX'S WEB SITE.

AND IF WE COULD PULL THAT UP, THE MODULE DATA SHEET. MDS, I THINK YOU CALLED IT, THE MODULE DATA SHEET. I THINK YOU CALLED IT MDS. NO, THE MODULE DATA SHEET. I THINK YOU CALLED IT MDS. AH, THERE WE GO.

THAT'S A DATA SHEET FOR A HYNIX UNBUFFERED DDR SDRAM DIMM. DIMM STANDS FOR, I BELIEVE, DUAL IN-LINE MEMORY MODULE, AND IT'S A PARTICULAR KIND OF MODULE, AND THIS ONE IS FOR DDR SDRAM IN PARTICULAR.

AND IF WE LOOK AT THE LAST PARAGRAPH IN THE DESCRIPTION, IT NOTES THAT -- NO, NO, BACK WHERE YOU WERE -- IN THE LAST PARAGRAPH IN THE DESCRIPTION, IT NOTES THAT THIS PARTICULAR MODULE INCORPORATES SOMETHING CALLED SERIAL PRESENCE DETECT, AND THAT'S A LITTLE BIT OF NON-VOLATILE MEMORY THAT'S ON THE MODULE SO THAT WHEN THE SYSTEM POWERS UP, THE CONTROLLER CAN TELL WHAT KIND OF MODULES IT HAS IN ITS MEMORY AND WHAT IT'S DEALING WITH.

AND IT READS THE INFORMATION SERIALLY FROM THE, FROM THIS LITTLE BIT OF NON-VOLATILE MEMORY THERE, IN THIS CASE, 2,048-BIT EEPROM.

AND IF WE COULD GO TO, I BELIEVE IT'S THE SECOND TO LAST PAGE WHICH DESCRIBES WHAT SORT OF INFORMATION IS AVAILABLE TO THE CONTROLLER -- KEEP GOING. IS THERE A FASTER WAY TO GET TO THE SECOND TO LAST PAGE? THERE WE GO. STOP. AND IF YOU COULD BLOW UP, I BELIEVE IT'S LINE 13 OF THESE, OF THE INFORMATION THAT'S CONTAINED IN THAT SERIAL

PRESENCE DETECT.

IT TALKS ABOUT THE PRIMARY DDR SDRAM WIDTH, AND IT SAYS IT'S BY 8, WHICH IS PROVIDING INFORMATION TO THE CONTROLLER ABOUT EXACTLY WHAT KIND OF CHIPS IT'S DEALING WITH, AND IN THIS CASE, FOR THIS PARTICULAR MODULE, THEY'RE BY EIGHT CHIPS. THEY EACH HAVE EIGHT DATA PINS.

SO, AGAIN, I DON'T THINK THE MODULES ARE RELEVANT.

TO THE EXTENT THEY ARE, THE CONTROLLER KNOWS EXACTLY WHAT IT'S DEALING WITH AND KNOWS HOW MUCH DATA IT'S GOING TO GET BACK FROM EACH CHIP.

MR. BROWN'S -- THIS CAN GO.

MR. BROWN'S SECOND POINT WAS ABOUT THE POSSIBILITY OF ISSUING OTHER COMMANDS TO INTERRUPT A BURST IN PROGRESS OR TO MASK IT.

WELL, I HAVE A FEW POINTS TO MAKE IN RESPONSE TO THAT.

FIRST, THE -- HYNIX'S CONSTRUCTION, RAMBUS'S PROPOSED CONSTRUCTION, AND THE COURT'S TENTATIVE CONSTRUCTION ALL TALK ABOUT THE AMOUNT OF DATA TO BE TRANSFERRED.

"TO BE TRANSFERRED" MUST HAVE SOME DIFFERENT MEANING FROM WHAT ACTUALLY IS TRANSFERRED.

"TO BE TRANSFERRED" IS THE AMOUNT THAT YOU WOULD TRANSFER IN THE NORMAL COURSE IF YOU DID NOT THEN ISSUE SOME OTHER COMMAND TO CUT OFF THAT BURST.

SECOND, MR. BROWN, I THINK, OVERSTATED THE AMOUNT OF DISCRETION HERE BASICALLY ON THE PART OF THE CONTROLLER IN VARIOUS RESPECTS, AND THESE ARE RELATIVELY MINOR POINTS, BUT I DO WANT TO JUST MENTION QUICKLY THAT THE DATA MASKING OPERATION THAT MR. BROWN WAS TALKING ABOUT, WHICH IS FOR BOTH READS AND WRITES IN SDRAMS, IS ONLY FOR WRITES IN DDR SDRAMS.

AND THAT'S MADE FAIRLY CLEAR IN HYNIX'S DDR SDRAM DATA SHEET, AND THIS IS EXHIBIT 68 TO MR. TAYLOR'S, ONE OF MR. TAYLOR'S DECLARATIONS.

IT'S AT PAGE 32 OF THAT DATA SHEET WHERE HE TALKS ABOUT DATA MASKING WRITE, AND IT SAYS, "DM COMMAND MASKS BURST WRITE DATA WITH REFERENCE TO DATA STROBE SIGNAL AND IT IS NOT RELATED WITH READ DATA."

IT'S NOT PERFECT ENGLISH, BUT IT MEANS THAT IT'S NOT AVAILABLE FOR READ COMMANDS FOR DDR SDRAMS, AND MR. TAYLOR TESTIFIED TO THAT IN HIS DEPOSITION.

MR. BROWN ALSO TALKED ABOUT THE PRECHARGE

COMMAND CUTTING OFF A READ BURST, BUT AS THE -- IN BOTH SDRAMS AND DDR COMMANDS, THE PRECHARGE COMMAND CAN -- MR. BROWN TALKED ABOUT THE PRECHARGE COMMAND AND ALSO THE BURST STOP COMMAND.

BUT IN BOTH DDR SDRAMS AND SDRAMS, INTERRUPTING BURSTS, WHETHER WITH A PRECHARGE OR A BURST STOP OR ANOTHER READ OR WRITE COMMAND IS NOT AVAILABLE FOR A READ WITH AUTO PRECHARGE.

AND IF WE COULD PULL UP THE SDRAM DEVICE OPERATION DOCUMENT? AND GO TO PAGE 7, AND BLOW UP THE TOP TEXT.

AT THE BOTTOM, IT NOTES HERE, "A READ OR WRITE COMMAND WITH AUTO PRECHARGE CANNOT BE TERMINATED BY READ, WRITE, PRECHARGE AND BURST STOP."

SO AT LEAST FOR THAT CLASS OF READ COMMAND, YOU CAN'T CHANGE THE BURST LENGTH ONCE YOU'VE ISSUED THE COMMAND IN THE WAY, IN SOME OF THE WAYS THAT MR. BROWN DESCRIBED.

BUT MR. BROWN ALSO SAID THAT IT WAS, YOU KNOW, "A FAIR SITUATION" I THINK ARE THE WORDS HE USED, WHEN A CONTROLLER WOULD ALWAYS WANT THE SAME NUMBER OF BITS.

I DON'T THINK THAT THERE'S ANY EVIDENCE IN THE RECORD TO SUPPORT THAT STATEMENT, AND I ALSO

DON'T THINK IT'S ACCURATE.

IN THE PROCESSORS THAT ARE IN USE TODAY, PRIMARILY BY AMD AND INTEL, THE PROCESSORS CONTAIN A CACHE, AND THERE'S A CERTAIN LENGTH OF CACHE LINE, AND TO EFFICIENTLY FILL THE CACHE LINE WITH DATA, A CERTAIN BURST LENGTH IS OPTIMAL.

AND IN FACT, THERE'S NO EVIDENCE IN THE RECORD ABOUT THIS EITHER, BUT IN FACT, IT IS THE CASE THAT DIFFERENT BURST LENGTHS OF FOUR AND EIGHT WERE SPECIFICALLY DEMANDED BY AMD AND INTEL SPECIFICALLY BECAUSE THEY WANTED THOSE OPTIMAL LENGTHS TO FILL THE DIFFERENT SIZES OF THEIR CACHE LINES IN THEIR PROCESSORS.

THE MAIN POINT I WANT TO MAKE, THOUGH, IS THAT EVEN THOUGH MR. BROWN OVERSTATES THE SITUATIONS IN WHICH YOU CAN INTERRUPT THESE BURSTS OR CUT THEM OFF OR CHANGE THEM, ALL THAT'S REALLY REQUIRED FOR INFRINGEMENT, AS WE POINTED OUT IN OUR PAPERS AND WE CITED CASES, IS THAT THE DEVICES BE REASONABLY CAPABLE OF PERFORMING IN AN INFRINGING MANNER.

AND THE DATA SHEETS SHOW THAT THEY ARE, AND MR. BROWN HIMSELF SHOWED AN EXAMPLE, THE TIMING DIAGRAM ON A DATA SHEET WHERE IT SHOWED A COMPLETE BURST. THAT'S HOW HYNIX REFERS TO BURSTS THAT ARE

NOT INTERRUPTED IN THEIR PAPERS.

THIS TIMING DIAGRAM THAT WE HAVE RIGHT HERE ON THE SCREEN SHOWS THAT. THE BURST LENGTH IS FOUR AND FOUR BITS OF DATA ARE COMING OUT.

AND MR. TAYLOR, AT HIS DEPOSITION, TESTIFIED TO THAT.

AND IF WE COULD PULL UP GRAPHIC NUMBER 64, WHICH IS A COUPLE OF QUOTES.

AND THE QUESTION WAS, "YOU GO ON IN YOUR DECLARATION TO TALK ABOUT THE POSSIBILITY IN THE HYNIX DEVICES OF INTERRUPTING BURSTS OF DATA WITH A BURST STOP COMMAND OR WITH A READ OR WRITE COMMAND; CORRECT?"

"ANSWER: A NEW LOAD OF DATA OR A NEW READ COMMAND, YES."

"QUESTION: OKAY. IS IT POSSIBLE FOR A USER TO OPERATE HYNIX'S DEVICES WITHOUT INTERRUPTING BURSTS OF DATA?"

"ANSWER: YES."

SIMILAR ANSWER WITH RESPECT TO MASKING DATA.

"QUESTION: IS IT POSSIBLE FOR A USER TO OPERATE HYNIX'S DEVICES WITHOUT MASKING DATA ON WRITES?"

"ANSWER: YES."

WE WERE SPECIFICALLY TALKING ONLY ABOUT WRITE DATA HERE BECAUSE MR. TAYLOR HAD TESTIFIED THAT THAT WAS ONLY AVAILABLE ON WRITES. I BELIEVE HE WAS THINKING OF DDR SDRAMS.

SO CLEARLY THE DEVICES ARE REASONABLY CAPABLE OF PERFORMING IN AN INFRINGING MANNER; THEREFORE, THEY INFRINGE.

THE COURT: OKAY. SHALL WE MOVE ON?

MR. BROWN: SURE. AND --

THE COURT: I DO WANT TO -- I SHOULD MENTION, WITH RESPECT TO RAMBUS'S MOTION, I DO WANT TO TALK ABOUT THE ONE THAT DEALS WITH A READ REQUEST.

MR. BROWN: WOULD YOU LIKE TO HEAR THAT NEXT?

THE COURT: SURE, WHY DON'T WE DO THAT NEXT?

MR. DETRE: SHOULD I GO FIRST ON RAMBUS'S MOTION?

THE COURT: SURE, SINCE YOU'RE THE MOVING PAPER, OR YOU'RE THE MOVING PARTY.

MR. DETRE: OKAY. WITH RESPECT TO READ REQUEST, WE HAVE AN AGREED CONSTRUCTION OF THE TERM. IT WAS THE CONSTRUCTION THAT WAS PROVIDED BY THE FEDERAL CIRCUIT.

AND IF WE COULD PULL UP NUMBER 66.

THIS IS WHAT THE FEDERAL CIRCUIT SAID: "FROM THE CORRECT PERSPECTIVE OF ONE OF SKILL IN THE ART AT THE TIME OF INVENTION, THE TERM 'READ REQUEST' MEANS A SERIES OF BITS USED TO REQUEST A READ OF DATA FROM A MEMORY DEVICE WHERE THE REQUEST IDENTIFIES WHAT TYPE OF READ TO PERFORM."

THE COURT: IS A READ REQUEST JUST A TYPE OF OPERATION CODE?

MR. DETRE: WELL, I THINK IT IS, YES, YOUR HONOR. I MEAN, I THINK BASICALLY, BASICALLY A READ REQUEST IS -- CAN BE CONSIDERED AN OPERATION CODE USED TO REQUEST A READ OF DATA.

THE COURT: AND DOESN'T REFERENCE TO SERIES OF BITS SUGGEST A PACKET PROTOCOL?

MR. DETRE: NO, I DON'T THINK IT DOES, YOUR HONOR.

HYNIX ARGUED THAT "SERIES OF BITS" DOES REFLECT A PACKET PROTOCOL BECAUSE THOSE BITS NEED TO -- THAT SERIES REPRESENTS A TIME SERIES AND THOSE BITS HAVE TO BE RECEIVED OVER MULTIPLE CLOCK CYCLES AS IN RAMBUS'S PACKETS, REQUEST PACKETS IN THE PREFERRED EMBODIMENT.

BUT IF WE ACTUALLY LOOK AT WHAT THE FEDERAL CIRCUIT WAS LOOKING AT WHEN THEY WERE

LOOKING AT THE READ REQUEST, THEY WERE, THEY WERE GUIDED BY THE SPECIFICATION -- THE EXAMPLES IN THE SPECIFICATION, WHICH -- AND THE PREFERRED EMBODIMENT THERE DOES INVOLVE PACKETS.

BUT THEY WERE -- I DON'T THINK THEY WERE IN ANY WAY TRYING TO RESTRICT RAMBUS TO THOSE, TO PACKETS.

AND, IN FACT, WHAT THEY IDENTIFIED WITH THE SERIES OF BITS IN THE PREFERRED EMBODIMENT WAS JUST ONE LITTLE PIECE OF ONE PACKET, FOUR BITS THAT ARE RECEIVED IN PARALLEL.

THEY'RE NOT A PACKET. THEY'RE JUST SOME BITS WHICH, IN THE PREFERRED EMBODIMENT WHICH DOES USE PACKETS, IS CONTAINED IN THE PACKET.

BUT THERE'S ABSOLUTELY NOTHING IN THE, IN THE CONSTRUCTION THAT THEY CAME UP WITH THAT SUGGESTS A PACKET.

THE COURT: WOULD YOU DEFINE FOR ME AGAIN A PACKET?

MR. DETRE: WELL, AS I SAID YESTERDAY, I THINK THAT THE TERM "PACKET" IS A SOMEWHAT VAGUE TERM.

BUT HYNIX SEEMS TO THINK, AT LEAST SOMETIMES, SOMETIMES IT SAYS THAT A PACKET NEEDS TO BE DEFINED EXACTLY AS A REQUEST PACKET IN THE

PREFERRED EMBODIMENT, AND SOMETIMES IT SEEMS TO IDENTIFY IT AS THE DISTINGUISHING FEATURE OF THE FACT THAT THERE IS SOME KIND OF PACKET PROTOCOL THAT ALLOWS YOU TO DETERMINE WHAT INFORMATION, WHAT KIND OF INFORMATION IS BEING TRANSMITTED TO THE DEVICE AT A GIVEN TIME.

IF WE --

THE COURT: OKAY. YOU TOLD ME HOW HYNIX WOULD DEFINE IT.

HOW WOULD YOU DEFINE IT?

MR. DETRE: WELL, I -- I'M NOT SURE THAT THERE IS A, THAT THE TERM "PACKET" IS ALWAYS USED CONSISTENTLY BY PEOPLE OF SKILL IN THE ART.

I DO THINK THAT WHEN PEOPLE REFER TO A PACKET, THEY DO THINK OF SOME SORT OF A PROTOCOL THAT ALLOWS IDENTIFICATION OF THE INFORMATION.

I DON'T THINK, AS HYNIX HAS SAID, THAT IT NEEDS TO BE TRANSMITTED OVER MULTIPLE CLOCK CYCLES OR VARIOUS OTHER SORTS OF LIMITATIONS THAT HAVE BEEN LOADED ONTO THAT TERM.

THE COURT: DO THE PATENTS IN ANY WAY -- OR IS THERE ANY EVIDENCE THAT THE SPECIFICATION WOULD SUGGEST TO ONE SKILLED IN THE ART THAT THE OPERATION CODE COULD BE TRANSMITTED OTHER THAN IN A PACKET?

MR. DETRE: WELL, I THINK -- I THINK SO, YOUR HONOR. I THINK THE ENTIRETY OF THE SPECIFICATION LAYS OUT MULTIPLE DISTINCT INVENTIONS AS THE PATENT OFFICE FOUND AND AS THE FEDERAL CIRCUIT HAS CONFIRMED.

AND ONE OF THOSE INVENTIONS DEALS WITH TRANSMITTING A REQUEST IN THAT, IN THE SORT OF PACKET FORMAT SHOWN IN THE PATENT.

BUT I DON'T THINK THERE'S ANYTHING IN THE PATENT --

(CELL PHONE RINGING IN THE AUDIENCE.)

THE COURT: LET ME JUST MAKE SURE EVERYBODY HAS TURNED OFF THEIR CELL PHONE.

MY RULE IS I DON'T LIKE IT THE FIRST TIME. THE SECOND TIME YOU'RE OUT OF HERE. SO JUST BEAR THAT IN MIND.

I DON'T MEAN TO BE MEAN, BUT IT IS A PROBLEM AND I NEED TO MAKE SURE IT'S DEALT WITH.

OKAY. GO AHEAD.

MR. DETRE: I DON'T THINK THERE'S ANYTHING IN THE PATENT TO SUGGEST THAT THE OTHER DISTINCT INVENTIONS THAT ARE NOT ABOUT THE PARTICULAR PACKETIZED PROTOCOL THAT SOME OF RAMBUS'S CLAIMS ARE DIRECTED TOWARDS, I DON'T THINK THERE'S ANYTHING IN THE PATENT TO SUGGEST THAT THE

OTHER DISTINCT INVENTIONS ARE RESTRICTED TO SENDING AN OPERATION CODE OR A READ REQUEST OR COMMANDS IN ANY PARTICULAR WAY.

A PERSON OF SKILL IN THE ART WOULD UNDERSTAND THAT YOU COULD SEND THOSE REQUESTS IN ANY WAY THAT, THAT -- BASICALLY IN ANY WAY KNOWN TO PEOPLE OF SKILL IN THE ART AND USE THESE DISTINCT INVENTIONS, LIKE MANY OF THE DISTINCT INVENTIONS WE'RE TALKING ABOUT HERE.

ACCESS TIME REGISTERS, THERE'S NOTHING ABOUT AN ACCESS TIME REGISTER THAT IS IN ANY WAY RESTRICTED TO A PARTICULAR METHOD OF TRANSMITTING A COMMAND.

BLOCK SIZE INFORMATION, AGAIN, NOTHING IN THAT THAT SUGGESTS IN ANY WAY THAT IT'S RESTRICTED TO A SPECIFIC WAY OF SENDING THE COMMAND TO THE DEVICE.

I THINK WHAT -- WHEN WE'RE DEALING HERE WITH AN APPLICATION, AN ORIGINAL APPLICATION THAT LAID OUT MULTIPLE DISTINCT INVENTIONS, I THINK THAT THE APPLICATION DESCRIBED IN SOME CASES IS BEING USED IN COMBINATION.

NEVERTHELESS, IT CAN -- IT CANNOT BE RESTRICTED TO JUST USING THOSE COMBINATIONS ALTOGETHER OR THERE WOULD BE ONLY ONE INVENTION.

AND THE INVENTIONS THAT ARE DISTINCT FROM THE PACKET, I DON'T THINK THERE'S ANYTHING IN THE PATENT TO SUGGEST THAT THEY SHOULD BE IN ANY WAY LIMITED TO OPERATION CODES SENT IN PACKETS.

I WOULD --

THE COURT: IS THERE ANY PARTICULAR LANGUAGE, OR IS IT JUST WHAT SOMEONE SKILLED IN THE ART WOULD KNOW AT THE TIME?

MR. DETRE: WELL, I THINK -- I THINK IT'S BOTH. THE ORIGINAL APPLICATION, OF COURSE -- AND IF WE'RE DISCUSSING HERE THE WRITTEN DESCRIPTION REQUIREMENT, YOUR HONOR --

THE COURT: I THINK, IN ESSENCE, WE ARE.

MR. DETRE: OKAY. THE ORIGINAL WRITTEN DESCRIPTION, OF COURSE, INCLUDES THE ORIGINAL CLAIMS.

THE COURT: RIGHT.

MR. DETRE: AND THERE'S NOTHING IN THE ORIGINAL CLAIMS THAT WOULD SUGGEST THAT ALL THE CLAIMS ARE DIRECTED TO PACKETS OR A PARTICULAR FORM OF SENDING OPERATION CODES IN PACKETS.

IF -- SOME OF THE ORIGINAL CLAIMS DID DISCUSS PACKETS. OTHERS DID NOT.

I THINK PRETTY CLEARLY ONE OF ORDINARY SKILL, LOOKING AT THAT WRITTEN DESCRIPTION,

INCLUDING THE MULTITUDE OF DISTINCT INVENTIONS DESCRIBED IN THE SPECIFICATION, FOLLOWED BY THE ORIGINAL CLAIMS, SOME OF WHICH DISCUSS PACKETS AND SOME OF WHICH DON'T, WOULD UNDERSTAND THAT THE ONES THAT DIDN'T WERE NOT RESTRICTED TO SENDING OPERATION CODES IN THAT WAY.

THE COURT: THEY DON'T EXPRESSLY TALK ABOUT A DIFFERENT WAY, DO THEY? THEY JUST DON'T SAY ONE WAY OR THE OTHER?

MR. DETRE: THEY DON'T -- EXCUSE ME, YOUR HONOR.

THEY DON'T EXPRESSLY TALK ABOUT A DIFFERENT WAY.

BUT IT'S -- THERE ARE A COUPLE OF, I THINK, PATENT LAW DOCTRINES THAT ARE VERY RELEVANT HERE. ONE IS THAT CLAIMS NEED NOT BE LIMITED TO A PREFERRED EMBODIMENT, EVEN IF THERE IS ONLY A SINGLE EMBODIMENT.

AND THE FEDERAL CIRCUIT HAS STATED THAT REPEATEDLY. FOR EXAMPLE, ONE OF THE CASES WE CITE IN OUR PAPERS, TELEFLEX VERSUS FICOSA, 299 F.3D AT 1313 AT 1325 MAKES THAT POINT.

WELL, OF COURSE, IF A CLAIM NEED NOT BE LIMITED TO A PREFERRED EMBODIMENT, EVEN IF THERE'S ONLY A SINGLE EMBODIMENT, THAT DOESN'T -- IT

FOLLOWS THAT, ALTHOUGH THAT WAS A CLAIM CONSTRUCTION CASE, OBVIOUSLY THE FEDERAL CIRCUIT WAS NOT SAYING, "BUT IF YOU CLAIM MORE BROADLY THAN A SINGLE EMBODIMENT, THEN YOU AUTOMATICALLY ARE NOT IN COMPLIANCE WITH THE WRITTEN DESCRIPTION REQUIREMENT."

THAT WOULDN'T MAKE SENSE. YOU'RE ALLOWED TO CLAIM MORE BROADLY.

SECOND, PATENTS NEED NOT TEACH THAT WHICH IS ALREADY KNOWN, AND A GOOD CITE FOR THAT IS INTEGRA LIFESCIENCES I, LIMITED VERSUS MERCK, 331 F.3D 860 AT 868.

AND THERE ARE OTHER CASES THAT SUGGEST THAT, IN FACT, A PATENT SHOULD NOT BELABOR WHAT IS ALREADY KNOWN BECAUSE IT JUST WOULD MAKE PATENT DOCUMENTS MUCH LONGER THAN THEY NEED TO BE.

THE KNOWLEDGE OF PEOPLE SKILLED IN THE ART IS ASSUMED HERE, AND ESPECIALLY IN THIS SORT OF CASE WHERE THERE ARE SO MANY DISTINCT INVENTIONS, TO TAKE ONE OF THEM AND READ IT INTO THE OTHERS WOULD NOT BE PROPER.

I'D LIKE TO ALSO PULL UP A QUOTE THAT I THINK IS RELEVANT FROM JUDGE NEWMAN IN THE REIFFIN VERSUS MICROSOFT CASE -- SLIDE NUMBER 68 -- IN WHICH SHE SAID IN THE CONCURRING OPINION, "IT IS

STANDARD FOR APPLICANTS TO PROVIDE CLAIMS THAT VARY IN SCOPE AND IN CONTENT, INCLUDING SOME ELEMENTS OF A NOVEL DEVICE OR METHOD, AND OMITTING OTHERS. CLAIMING AN INVENTION IN THIS MANNER DOES NOT RAISE AN ISSUE OF COMPLIANCE WITH SECTION 112, PARAGRAPH 1," THE WRITTEN DESCRIPTION REQUIREMENT.

SO I THINK IT IS QUITE CLEAR THAT FOR THOSE INVENTIONS THAT ARE NOT ABOUT PACKETS, FOR THOSE INVENTIONS, THE KNOWLEDGE OF A PERSON OF ORDINARY SKILL IS ASSUMED, AND THAT PERSON OF ORDINARY SKILL WILL KNOW VARIOUS WAYS TO TRANSMIT OPERATION CODES TO THE DEVICES.

THERE'S NOTHING IN THE PATENT -- THE FEDERAL CIRCUIT, WHEN READING IN LIMITATIONS FROM CERTAIN EMBODIMENTS, HAS REQUIRED AN UNAMBIGUOUS DISCLOSURE IN THE PATENT THAT THIS IS THE ONLY WAY TO PERFORM THIS PARTICULAR INVENTION.

THAT'S, FOR EXAMPLE, IN THE GENTRY GALLERY CASE WHICH HAS, TO A LARGE EXTENT, BEEN DISCREDITED TO THE EXTENT THAT HYNIX SAYS.

BUT TO THE EXTENT THAT IT'S STILL GOOD LAW --

THE COURT: I DON'T THINK THEY REALLY DISAGREE WITH YOU ON WHAT THAT CASE SAYS.

MR. DETRE: WELL, PERHAPS NOT AS

EVIDENCED BY THEIR REPLY BRIEF.

THE COURT: RIGHT.

MR. DETRE: ALTHOUGH IN THEIR REPLY BRIEF, I THINK, AND IN SOME OF THEIR MOTIONS, HYNIX, WHILE AGREEING THAT THE ESSENTIAL ELEMENT TEST HAS BEEN DISCREDITED, STILL SEEMS TO BE URGING THAT VARIOUS FEATURES IN RAMBUS'S SPECIFICATION ARE AN ESSENTIAL ELEMENT AND, THEREFORE, MUST BE IN ALL OF THE CLAIMS.

I DON'T THINK THAT CAN BE SQUARED WITH THE VARIOUS RESTRICTION REQUIREMENTS ISSUED BY THE PTO, WHICH SEPARATE OUT VARIOUS INVENTIONS.

THE NUMBER OF PATENTS THAT HAVE ISSUED CLAIMING VARIOUS DIFFERENT INVENTIONS, THE STATEMENT OF THE FEDERAL CIRCUIT THAT THERE ARE MANY INVENTIONS DISCLOSED, ALL OF THAT SUGGESTS THAT YOU'VE GOT A LARGE NUMBER OF DISTINCT INVENTIONS, THE ONES THAT DO NOT SPECIFICALLY CALL OUT SOME SORT OF A PACKETIZED PROTOCOL DO NOT, DO NOT DEPEND ON IT AND A PERSON OF ORDINARY SKILL WOULD UNDERSTAND THAT.

AND AGAIN, THE SPECIFICATION SIMPLY DOES NOT NEED TO TEACH THAT WHICH IS ALREADY KNOWN.

IF WE COULD GO --

THE COURT: I DIDN'T MEAN TO STEER YOU

OFF OUR SUBJECT.

MR. DETRE: WELL, I THINK THAT WAS PROBABLY AN IMPORTANT SUBJECT TO DISCUSS, YOUR HONOR.

GOING BACK TO WHAT THE FEDERAL CIRCUIT ACTUALLY LOOKED AT WHEN IT WAS CONSTRUING READ REQUEST, IT DID LOOK AT THE PREFERRED EMBODIMENT IN THE SPECIFICATION.

AND IF WE COULD PULL UP NUMBER 65.

AND IT LOOKED AT FIGURE 4 OF THE '918 PATENT, WHICH SHOWS A REQUEST PACKET.

BUT THE POINT OF DISPUTE BEFORE THE FEDERAL CIRCUIT WAS THAT INFINEON WAS ARGUING THAT A READ REQUEST REALLY HAS TO BE THIS WHOLE REQUEST PACKET. IT HAS TO INCLUDE ALL THE THINGS, ALL OF THE INFORMATION NECESSARY FOR A READ OPERATION, THE ADDRESS, THE BLOCK SIZE AND SO FORTH.

AND RAMBUS WAS MAKING THE POINT, NO, THAT'S NOT RIGHT. THE READ REQUEST IN THE PREFERRED EMBODIMENT, THE READ REQUEST ONLY CORRESPONDS TO THE FOUR BITS OF THE ACCESS TYPE, AND THAT'S SHOWN AT THE TOP, ACCESS TYPE 0 TO 3. THAT'S FOUR BITS, 0, 1, 2, 3.

THOSE BITS, WHILE IN THIS PARTICULAR PREFERRED EMBODIMENT, ARE TRANSMITTED IN THE

PACKET. THERE'S NO REASON WHY FOUR BITS LIKE THAT NEED TO BE TRANSMITTED IN THE PACKET.

HYNIX'S MAIN ARGUMENT IN ITS PAPERS IS THAT A PACKET, I DON'T THINK THIS IS NECESSARILY TRUE, BUT THEY SAY THAT A PACKET NEEDS TO BE RECEIVED OVER MULTIPLE CLOCK CYCLES BECAUSE THAT'S THE FORM THAT A PACKET TAKES IN RAMBUS'S PREFERRED EMBODIMENT.

WELL, THOSE FOUR BITS ARE NOT RECEIVED ON THE MULTIPLE CLOCK CYCLES. THEY ARE RECEIVED, IN THIS CASE, OVER ONE BUS CYCLE, WHICH IN THE RAMBUS PREFERRED EMBODIMENT IS HALF A CLOCK CYCLE. THEY'RE ALL RECEIVED IN PARALLEL.

AND THE FEDERAL CIRCUIT, ON THIS POINT, SIDED WITH RAMBUS. THEY SAID THAT THAT'S RIGHT, THAT A READ REQUEST DOESN'T NEED TO BE THE WHOLE PACKET. IN THE PREFERRED EMBODIMENT, THE READ REQUEST DOES CORRESPOND TO THESE FOUR BITS OF THE ACCESS TYPE.

AND THEN BASED ON THAT, THEY CAME UP WITH THEIR CONSTRUCTION.

NUMBER 66, AGAIN, IF WE COULD GO BACK TO THAT.

NOW, OBVIOUSLY IF THE FEDERAL CIRCUIT HAD MEANT TO RESTRICT THIS TO A PACKET, THEY COULD HAVE

SAID, "THE TERM 'READ REQUEST' CONTAINS A SERIES OF BITS CONTAINED IN A PACKET."

THEY DID NOT SAY SO. THEY JUST SAID A SERIES OF BITS. THEY USED QUITE GENERAL LANGUAGE.

WHAT THEY WERE LOOKING AT WHEN THEY SAID THAT WAS THIS PARTICULAR FOUR BITS IN THIS REQUEST PACKET, WHICH WAS THE EXAMPLE IN THE PREFERRED EMBODIMENT.

BUT THEY, IN NO WAY IN THE LANGUAGE THEY CHOSE, RESTRICTED IT TO THAT.

SO FIRST THEY DID NOT RESTRICT IT TO A PACKET IN THE LANGUAGE THEY CHOSE.

SECOND, THE EXAMPLE THAT THEY WERE CONSIDERING SHOWS THAT HYNIX'S ARGUMENT CANNOT BE CORRECT THAT WHEN THEY SAID A SERIES OF BITS, THEY MEANT RECEIVED OVER MULTIPLE CLOCK CYCLES, BECAUSE THE EXAMPLE THAT THEY DISCUSSED AND THAT WAS ONE OF THE FACTORS THAT EVENTUALLY LED THEM TO THEIR CONSTRUCTION DIDN'T HAVE THE PARTICULAR SERIES OF BITS RECEIVED OVER MULTIPLE CLOCK CYCLES.

I THINK THE OTHER, THE OTHER MAIN ARGUMENT THAT HYNIX MAKES WITH RESPECT TO WHY ITS ACCUSED DEVICES DO NOT INFRINGE, OTHER THAN THE SERIES OF BITS POINT, IS THAT IN THEIR DEVICES, THEIR READ COMMANDS, OR READ REQUESTS, DO NOT

IDENTIFY WHAT TYPE OF READ TO PERFORM.

AND AS WE POINTED OUT IN OUR PAPERS, HYNIX'S DATA SHEETS VERY CLEARLY IDENTIFY TWO TYPES OF READ COMMANDS: READ AND READ WITH AUTO PRECHARGE.

AND IN MR. BROWN'S TUTORIAL, ONE OF HIS GRAPHICS, IN FACT, VERY CLEARLY SHOWED THOSE TWO TYPES.

IF WE COULD PULL UP PAGE 24 OF THE TUTORIAL.

AND YOU'LL SEE HERE, YOUR HONOR, THAT THERE ARE TWO READ COMMANDS SHOWN THAT MR. BROWN IDENTIFIED, BOTH DESIGNATED AS RD.

BUT ON THE FIRST READ COMMAND, IF WE FOLLOW THAT DOWN, ON THE FIRST READ COMMAND, THE A10 LINE HERE IS LOW, AND ON THE SECOND READ COMMAND, THE A10 LINE IS HIGH.

AND ON THIS ONE, IN FACT, IT'S HARD TO READ HERE, BUT THIS ONE IS IDENTIFIED, THE SECOND ONE, AS A READ WITH AUTO PRECHARGE.

THE FIRST ONE IS JUST A READ WITHOUT AUTO PRECHARGE.

SO THERE ARE SHOWN ON THIS PARTICULAR TIMING DIAGRAM TWO TYPES OF READS IDENTIFIED.

YOU KNOW, MR. BROWN, OVER ON THE

LEFT-HAND SIDE, HAS BRACKETED JUST THE FIRST FOUR CONTROL SIGNALS.

BUT THE A10 BIT IS ALSO PART OF BOTH OF THOSE READ OPERATIONS IDENTIFYING WHETHER IT'S A READ WITHOUT AUTO PRECHARGE OR A READ WITH AUTO PRECHARGE.

HYNIX HAS ARGUED THAT THOSE ARE NOT REALLY TWO DIFFERENT TYPES OF READS BECAUSE ESSENTIALLY YOU'LL GET THE SAME DATA BACK WHETHER IT'S A READ WITHOUT AUTO PRECHARGE OR A READ WITH AUTO PRECHARGE.

I THINK THERE ARE A COUPLE OF RESPONSES TO THAT. ONE GOES BACK, AGAIN, TO WHAT THE FEDERAL CIRCUIT WAS CONSIDERING WHEN IT CAME UP WITH ITS CONSTRUCTION WHICH SAID THAT THE READ REQUEST IDENTIFIES THE TYPE OF READ TO PERFORM.

AND IF WE COULD GO AGAIN TO NUMBER 65.

THE FEDERAL CIRCUIT DID LOOK AT THE PREFERRED EMBODIMENT, CONSTRUED THE TERM IN LIGHT OF THE PREFERRED EMBODIMENT, AND SAID THAT IN THE -- AT THE BOTTOM OF THIS LITTLE QUOTE FROM THE FEDERAL CIRCUIT DECISION, LOOKING AT THE ACCESS TYPE, THAT FOUR-BIT FIELD THAT, IN THE PREFERRED EMBODIMENT, IS THE READ REQUEST, THE FEDERAL CIRCUIT SAID, THE LAST LINE HERE, "THE FIRST BIT

INSTRUCTS THE MEMORY DEVICE TO PERFORM A READ; THE NEXT THREE BITS TELL THE DEVICE WHAT TYPE OF READ TO PERFORM (E.G. PAGE READ, NORMAL ACCESS READ, ET CETERA)."

AND I THINK IT'S INSTRUCTIVE TO LOOK AT WHAT THAT E.G. AND THAT ET CETERA MEANT WHEN THE FEDERAL CIRCUIT WAS DISCUSSING THE TYPE OF READ SPECIFIED BY THE ACCESS TYPE.

IF WE COULD GO TO THE '263 PATENT AND GO TO PAGE 21, AND UP TOWARDS THE TOP OF COLUMN 10. THERE YOU GO, JUST BLOW THAT UP. GO A LITTLE BIT FURTHER DOWN. STOP THERE.

AFTER TALKING ABOUT THE ACCESS TYPE IN THE PREVIOUS PARAGRAPH, THE FEDERAL CIRCUIT -- SORRY, EXCUSE ME.

THE PATENT SPECIFICATION NOTES, "THE METHOD OF THIS INVENTION PROVIDES FOR ACCESS MODE CONTROLS SPECIFICALLY FOR THE DRAMS. ONE SUCH ACCESS MODE DETERMINES WHETHER THE ACCESS IS PAGE MODE OR NORMAL RAS ACCESS."

AND THAT'S THE PARTICULAR EXAMPLE OF A TYPE THAT THE FEDERAL CIRCUIT MENTIONED IN ITS OPINION, BUT IT SAID THAT THAT WAS AN EXAMPLE AND THEN IT PUT IN THE ET CETERA.

AND IF WE COULD GO DOWN TO THE NEXT

PARAGRAPH, THE VERY BEGINNING OF THE NEXT PARAGRAPH IN COLUMN 10. NO, NO, THE NEXT ONE. THERE.

"THE ACCESS MODE ALSO DETERMINES WHETHER THE DRAM SHOULD PRECHARGE THE SENSE AMPLIFIERS OR SHOULD SAVE THE CONTENTS OF THE SENSE AMPS."

THAT WAS ANOTHER TYPE OF READ SPECIFICALLY DESIGNATED BY A BIT IN THAT ACCESS TYPE FIELD THAT, IN THE PREFERRED EMBODIMENT, CORRESPONDS TO READ REQUEST.

AND IF WE COULD GO TO THE NEXT PAGE, PAGE 22, IT'S MADE PERHAPS EVEN CLEARER THERE.

ON COLUMN 11 WHERE YOU SEE THAT TABLE, IF YOU BLOW UP THE TABLE AND GO A FEW LINES UNDERNEATH IT. KEEP GOING, KEEP GOING. STOP.

IF WE LOOK UNDER THE TABLE A FEW LINES DOWN, IT SAYS ACCESS TYPE BIT NUMBER TWO, THAT'S THE PAGE MODE/NORMAL SWITCH, AND ACCESS TYPE BIT MODE NUMBER 3, THAT'S THE PRECHARGE/SAVE-DATA SWITCH.

AND THAT PRECHARGE SAVE-DATA SWITCH IS EXACTLY WHAT CORRESPONDS TO WITH OR WITHOUT AUTO PRECHARGE ACCORDING TO HOW THAT BIT IS SET, SIMILAR TO HOW THE A10 BIT IS SET IN HYNIX'S DEVICES, THE PRECHARGE WILL OR WILL NOT TAKE PLACE AS PART OF THE READ OPERATION.

HYNIX ALSO OVERSTATES THE CASE WHEN IT SAYS THAT THE READ OPERATION, THE DATA THAT'S READ OUT WILL NOT BE AFFECTED BY WHETHER YOU DO IT WITH OR WITHOUT A PRECHARGE.

AND WE LOOKED AT THIS JUST BEFORE, IT'S ACTUALLY ON ANOTHER POINT, BUT IF WE COULD PULL UP THE SDRAM DEVICE OPERATION, AND GO TO PAGE 7 AND BLOW UP THE TOP PART, THE TEXT UNDER AUTO PRECHARGE, AND BLOW UP THE TIMING DIAGRAM, TOO, PLEASE.

WELL, WE NOTICE A COUPLE OF THINGS. ONE IS THAT THE AUTO PRECHARGE START OCCURS WHILE THE READ DATA IS STILL COMING OUT. IT STARTS TO PRECHARGE DURING THE READ OPERATION.

AND SECOND, WHAT I POINTED OUT BEFORE, A READ OR WRITE COMMAND WITH AUTO PRECHARGE CANNOT BE TERMINATED IN THE WAY THAT READ COMMANDS WITHOUT AUTO PRECHARGE CAN BE.

SO, IN SHORT, THIS IS EXACTLY THE TYPE OF READ THE FEDERAL CIRCUIT WAS LOOKING AT WHEN IT -- THIS IS ONE OF THE TYPES OF READS THE FEDERAL CIRCUIT WAS LOOKING AT WHEN IT CAME UP WITH ITS CONSTRUCTION.

THAT'S NOT IN ANY WAY TO SUGGEST THAT THE FEDERAL CIRCUIT'S CONSTRUCTION IS RESTRICTED TO THE

PREFERRED EMBODIMENT, BUT IT SHOULD AT LEAST INCLUDE IT GIVEN THAT THEY WERE LOOKING AT IT.

AND SECOND, HYNIX'S OWN DOCUMENTS CLEARLY SHOW THAT THESE ARE TWO DIFFERENT TYPES OF READS.

THE COURT: OKAY.

MR. BROWN: THERE'S A LOT TO ADDRESS HERE, YOUR HONOR, AND I WILL TRY AND DO IT IN A RELATIVELY ORGANIZED FASHION.

THE COURT: OKAY.

MR. BROWN: THIS IS THE AGREED DEFINITION, THE DEFINITION WHICH WAS ANNOUNCED BY THE FEDERAL CIRCUIT.

THE FEDERAL CIRCUIT DID NOTE IN ITS OPINION THAT RAMBUS SAID THAT THE READ REQUEST WAS THE SAME AS THE OPERATION CODE.

THE FEDERAL CIRCUIT DID NOT ADOPT RAMBUS'S DECISION.

INSTEAD, THEY CAME UP WITH THIS DECISION, WITH THIS CONSTRUCTION OF THE TERM "READ REQUEST."

NOW, I DO NOT THINK THAT THIS REQUIRES NECESSARILY THAT IT, THAT THE READ REQUEST BE IN A PACKET.

BUT I'M GOING -- I TAKE THE FEDERAL CIRCUIT AT FACE VALUE THAT IT DOES REQUIRE THAT A READ REQUEST BE A SERIES OF BITS. IT MIGHT NOT BE

IN A PACKET. IT MIGHT BE, YOU KNOW, ONE BIT OR, YOU KNOW, A COUPLE OF BITS IN ONE CLOCK CYCLE AND THEN SOME NUMBER OF CLOCK CYCLES LATER, IT MIGHT BE ANOTHER NUMBER OF BITS, SOMETHING LIKE THAT.

BUT IT HAS TO BE A TIMED SERIES OF BITS, AND THERE'S NO BASIS, IN MY VIEW, FOR SAYING THAT A SERIES CAN BE A READ COMMAND, EVEN WITH THE A10 BIT.

THE READ COMMAND IS THE COMMAND ON RAS, CAS, WRITE ENABLED CHIP SELECT, AND EVEN INCLUDING THE A10 BIT, THEY ALL ARE READ IN SIMULTANEOUSLY.

THAT'S THE ONLY THING THAT RAMBUS HAS ACCUSED OF BEING A READ REQUEST, AND I ASSUME THAT THERE IS GOOD REASON WHY THEY HAVE DONE THAT.

BUT THERE IS NO WAY THAT THOSE, EVEN IF YOU SAY ALL FIVE BITS ARE A PART OF THE READ REQUEST, THAT THOSE ARE IN SERIES, OKAY.

AND I DON'T THINK -- I DON'T THINK THAT THE FEDERAL CIRCUIT NECESSARILY MEANT THAT IT HAD TO BE IN A PACKET.

BUT I THINK IT IS VERY CLEAR THAT THE FEDERAL CIRCUIT HAD IN MIND THAT IT WAS A SERIES OF BITS, AND THEY NOTED RAMBUS'S CONTENTION AS TO WHAT A READ REQUEST MEANT AND THEY REJECTED IT AND INSTEAD THEY CAME UP -- AND THEY CAME UP WITH THIS

CONSTRUCTION.

NOW, I'M NOT GOING TO DO A LOT OF SPECULATION HERE AS TO HOW THE FEDERAL CIRCUIT ARRIVED AT THIS PARTICULAR CONSTRUCTION BECAUSE I'M NOT SURE THAT THERE'S A LOT OF EXPLANATION OF HOW THEY CAME UP WITH THIS, AND MANY OF RAMBUS'S EXPLANATIONS OF HOW THE FEDERAL CIRCUIT REACHED THIS DECISION ARE JUST PURE SPECULATION.

HOWEVER, I WILL TAKE THE FEDERAL CIRCUIT AT FACE VALUE ON THIS WITH A CONSTRUCTION WHICH IS BINDING ON RAMBUS THAT IT DOES REQUIRE A SERIES -- THAT A READ REQUEST DOES REQUIRE A SERIES OF BITS, AND I DON'T THINK THAT THERE IS ANY SUPPORTABLE POSITION THAT A SERIES OF BITS COULD BE ANYTHING MORE OR ANYTHING LESS THAN BITS THAT COME IN AT DIFFERENT TIMES.

THEY MAY NOT HAVE TO BE, YOU KNOW, ONCE A CLOCK CYCLE. THEY MAY NOT HAVE TO BE ONE BIT PER CLOCK CYCLE OR ONE BIT AT A TIME, BUT THERE DOES HAVE TO BE A TIME SEQUENCE OF BITS INPUT.

SECOND. YES, THE FEDERAL CIRCUIT SAYS THE REQUEST HAS TO IDENTIFY WHAT TYPE OF READ TO PERFORM, NOT WHAT KIND OF ACCESS, NOT WHAT KIND OF MODE TO, TO PUT THE MEMORY INTO, BUT WHAT TYPE OF READ TO PERFORM.

AND THE -- IT'S VERY CLEAR FROM THE FEDERAL CIRCUIT OPINION THAT THE ONLY TWO TYPES OF READS THAT WERE ACTUALLY IDENTIFIED IN THAT OPINION ARE A NORMAL MODE READ AND A PAGE MODE READ, AND THOSE ARE TWO DIFFERENT TYPES OF READS BECAUSE, IF YOU REMEMBER LAST THURSDAY, WE -- IN THE TUTORIAL WE TALKED BRIEFLY ABOUT WHAT THE DIFFERENCE IS BETWEEN A NORMAL MODE READ AND A PAGE MODE READ, AT LEAST WITHIN THE CONTEXT OF THE PREFERRED EMBODIMENT OF THE PATENTS.

AND IN A NORMAL -- A REQUEST PACKET HAS THE SAME FORMAT IN BOTH OF THOSE CASES.

BUT IN THE NORMAL MODE READ, THE DEVICE, THE MEMORY DEVICE HAS TO KNOW TO FIRST EXTRACT THE ROW ADDRESS, ACTIVATE THE ROW, THEN USING A COLUMN ADDRESS EXTRACTED FROM THE PACKET, CHOOSE THE BITS FROM THE PARTICULAR COLUMNS. THAT'S A NORMAL MODE READ.

NOW, IN A PAGE MODE READ, THE PACKET HAS THE SAME REQUEST FORMAT, BUT BASICALLY BECAUSE THERE IS A ROW ALREADY OPEN, THE PACKET -- OR THE MEMORY CHIP NEEDS TO KNOW JUST TO EXTRACT THE COLUMN ADDRESS, USE THAT COLUMN ADDRESS TO SELECT THE BITS TO COME FOR OUTPUT.

BUT BECAUSE, AGAIN, IN THE PREFERRED

EMBODIMENT, BECAUSE THE PACKET HAS THE SAME FORMAT FOR WHETHER IT'S A PAGE MODE READ OR A NORMAL MODE READ, THAT IS, IT HAS THE SAME, BASICALLY THE SAME NUMBER OF BITS IN THE ADDRESS IN THE PACKET, THE PACKET HAS TO TELL THE MEMORY CHIP WHETHER THIS IS A NORMAL MODE READ OR WHETHER THIS IS A PAGE MODE READ, AND THOSE ARE THE ONLY TYPES OF READS THAT WERE MENTIONED IN THE FEDERAL CIRCUIT OPINION.

NOW, YES, THE FEDERAL CIRCUIT USED AN E.G. AND THEY USED AN ET CETERA.

OKAY. BUT THEY DIDN'T TELL US -- UNLIKE RAMBUS'S SPECULATION, THEY DIDN'T TELL US WHAT THAT ET CETERA MEANT.

AND IF YOU GO BACK TO WHAT MR. DETRE TOLD YOU FROM THE, OR POINTED OUT FROM THE, FROM THE '263 PATENT, BASICALLY HE WAS TALKING ABOUT ACCESS MODE CONTROL, AND THOSE THREE BITS THAT HE'S USING, YES, ARE USED IN ACCESS MODE CONTROL.

BUT AN ACCESS MODE IS NOT THE SAME AS A TYPE OF READ. THERE'S NO -- I MEAN, THIS IS BASICALLY -- THE ACCESS MODE CONTROL IS CONTROLLING THE OPERATIONS THAT ARE GOING TO OCCUR DURING WHATEVER ACCESS IS BEING REQUESTED.

IN ONE OF THOSE, ONE OF THOSE THINGS IN THE RAMBUS PATENT, AND ACTUALLY THERE'S AN ANALOGY

IN THE SDRAM WHICH I'M GOING TO COME TO IN JUST A MINUTE, BUT BASICALLY THERE ARE TWO TYPES OF READS THAT ARE SPECIFIED. THERE'S A NORMAL MODE AND THERE'S A PAGE MODE. THERE'S AT LEAST THOSE.

NOW, THE ACCESS MODE, ONE OF THESE BITS, ALSO SAYS AFTER YOU'RE DONE WITH THIS READ, PRECHARGE OR SAVE THE DATA.

OKAY. IT BASICALLY -- PART OF THIS ACCESS MODE CONTROL IS TO TELL THE CHIP WHAT TO DO AFTER THE READ OPERATION IS COMPLETE.

AND THAT'S WHAT HAPPENS IN SDRAMS ALSO, OKAY, THIS A10 BIT. IT BASICALLY SAYS WHAT TO DO AFTER THE READ OPERATION IS COMPLETE.

AND THE SLIDE FROM MY TUTORIAL THAT MR. DETRE SHOWED YOU -- AND I MAY EVEN ACTUALLY BE ABLE TO FIND IT -- I THINK THIS IS THE ONE THAT MR. DETRE SHOWED YOU, OKAY, THAT, YES, THERE'S A READ BANK -- THERE'S ONE READ COMMAND THAT'S JUST A READ WITH THE A10 BIT INACTIVE, AND THEN THERE'S ANOTHER READ COMMAND WITH THE A10 BIT ACTIVE, OKAY, WHICH MR. DETRE IS BASICALLY INDICATING IS A READ WITH AUTO PRECHARGE, OKAY.

IT CERTAINLY LOOKS TO ME AS IF THE DATA THAT COMES OUT IN RESPONSE TO THOSE TWO READ COMMANDS IS PRETTY MUCH THE SAME.

THE DIFFERENCE OF THE A10 BIT IS THAT AFTER THE READ OF DATA IS COMPLETED, IT SPECIFIES ANOTHER OPERATION THAT SHOULD OCCUR AFTER THAT POINT. IT DOESN'T CHANGE THE TYPE OF READ.

AND I CAN ILLUSTRATE THAT. THERE ARE TWO WAYS OF DOING THIS, OKAY, AND THIS IS -- THE TOP DIAGRAM IS THE ONE THAT MR. DETRE TOLD YOU, OR SHOWED YOU, FOR ONE OF THE TIMING DIAGRAMS, AND IT IS THAT YOU COULD SEND A BURST READ WITH AUTO PRECHARGE, AND THIS BASICALLY IS A READ COMMAND, SIMULTANEOUSLY WITH THE FOUR BITS IN THE READ COMMAND, AND THE A10 BIT IS SECOND. OKAY. SO THAT BECOMES A READ WITH AUTO PRECHARGE OPERATION.

NOW, YOU CAN DO EXACTLY THE SAME THING WITH TWO SEPARATE COMMANDS. YOU CAN SEND IN THE READ COMMAND WITH THE A10 BIT NOT SET, AND THEN JUST BEFORE THE END OF THE BURST, YOU SEND A PRECHARGE COMMAND AND EXACTLY THE SAME THING HAPPENS.

BUT INSTEAD WHAT YOU'VE DONE IS YOU'VE COMMANDED ONE OPERATION WITH THE READ COMMAND AND YOU'VE COMMANDED ANOTHER OPERATION WITH THE PRECHARGE COMMAND.

WHEN YOU SEND IN A READ WITH THE A10, OR A READ COMMAND WITH THE A10 BIT SET, YOU'RE

BASICALLY TELLING THE DEVICE TO DO TWO OPERATIONS, FIRST DO THE READ, THEN DO THE PRECHARGE.

OKAY. SO THE A10 BIT, IN OUR VIEW, IN HYNIX'S VIEW, DOES NOT -- IT IS NOT SOMETHING THAT SPECIFIES A TYPE OF READ TO PERFORM, AND THAT'S NOT INCONSISTENT WITH EITHER THE PATENT SPECIFICATION OR WITH THE FEDERAL CIRCUIT'S, THE FEDERAL CIRCUIT'S DISCUSSION.

NOW, I DO WANT TO GO BACK AND ANSWER A QUESTION THAT I DIDN'T HEAR MR. DETRE ANSWER. THERE IS NO DISCLOSURE IN THE PATENT OF AN OP CODE BEING TRANSMITTED TO THE DEVICE IN ANY WAY OTHER THAN WITHIN A PACKET. THERE'S NO SUGGESTION THAT AN OP CODE CAN BE TRANSMITTED IN ANY WAY OTHER THAN THE PACKET.

AND MR. DETRE IS CORRECT THAT YOU DON'T HAVE TO DISCLOSE EVERYTHING THAT IS KNOWN.

BUT THE RELEVANT INQUIRY UNDER SECTION 112 IS WHETHER OR NOT THE INVENTION, AS CLAIMED, OKAY, THAT IS IN THE GRANTED CLAIM AND WHICH IS THE GRANTED CLAIM AS CONSTRUED BY THE COURT, WHETHER THAT IS DISCLOSED IN THE SPECIFICATION, EITHER EXPRESSLY OR INHERENTLY.

AND IF YOU DIVORCE -- THERE IS NO DISCLOSURE OF AN OPERATION CODE OUTSIDE OF THE USE

OF A PACKET.

AND MR. MURPHY AGREED WITH THAT IN HIS -- IT'S HERE SOMEWHERE. MR. MURPHY AGREED WITH THAT IN HIS DEPOSITION.

"IS THERE ANY DISCLOSURE IN THE PATENT OF AN OPERATION CODE THAT IS NOT CONTAINED IN A PACKET?"

AND HE AGREED THAT IN THE PREFERRED EMBODIMENT, ALL OF THE OP CODES ARE DELIVERED OVER THE -- OR DELIVERED IN A PACKET.

NOW, HE ALSO SAYS THAT HE BELIEVES ONE OF ORDINARY SKILL IN THE ART WOULD UNDERSTAND THAT IT DOESN'T HAVE TO BE DELIVERED IN A PACKET.

BUT ON THE OTHER HAND, THERE'S NO OTHER WAY, THERE'S NO DISCLOSURE IN THE PATENT, AND MR. MURPHY AGREED THAT THERE'S NO DISCLOSURE OF AN OP CODE BEING DELIVERED IN SOME WAY OTHER THAN IN A PACKET.

NOW, SO IN ORDER TO MEET THE WRITTEN DESCRIPTION REQUIREMENT, THERE HAS TO BE SOME DISCLOSURE. IT'S EITHER EXPRESS OR BY PRINCIPLES OF INHERENCE, NOT -- OR BY PRINCIPLES OF INHERENCY THAT THE INVENTION AS CLAIMED, AS NOW CLAIMED, THAT IS THE OPERATION DIVORCED FROM A PACKET, OKAY, IS BASICALLY WHAT THEY'RE SAYING A CLAIM IS NOW, OKAY,

WAS IN POSSESSION OF THE INVENTORS AT THE TIME OF THE ORIGINAL FILING.

AND THERE IS NO SUCH DISCLOSURE.

THE MOST THAT RAMBUS CAN SAY IS, FROM OUR DISCLOSURE OF AN OPERATION CODE IN A PACKET, IT'S OBVIOUS TO ONE OF ORDINARY SKILL IN THE ART THAT THE OPERATION CODE CAN BE DELIVERED IN OTHER WAYS.

BUT THAT'S NOT THE TEST. THE FEDERAL CIRCUIT HAS SAID IN LOCKWOOD VERSUS AMERICAN AIRLINES, HAS SAID IN DELAVAL V. GENERAL ELECTRIC, THAT WHETHER SOMETHING IS OBVIOUS IN VIEW OF THE DISCLOSURE IS NOT THE CORRECT TEST UNDER THE WRITTEN DESCRIPTION REQUIREMENT.

THERE HAS TO BE A DISCLOSURE WHICH IS EXPRESS OR WHICH IS INHERENT.

AND YES, IT'S A DISCLOSURE AS VIEWED BY ONE OF ORDINARY SKILL IN THE ART, BUT THE, THE DISCLOSURE HAS TO BE IN THE SPECIFICATION.

THE COURT: SO UNDER THE WRITTEN DESCRIPTION REQUIREMENT, IF SOMEONE READING A PATENT, IF EVERYBODY WOULD KNOW, "OH, THIS SAYS IT NEEDS TO BE IN, OR IT IS IN A PACKET, BUT WE ALL KNOW YOU CAN DO IT OTHERWISE," THAT WRITTEN DESCRIPTION IS INSUFFICIENT TO SUPPORT IT?

MR. BROWN: THERE HAS TO BE SOMETHING IN

THE WRITTEN DESCRIPTION, IN THE WRITTEN DESCRIPTION THAT SAYS, YOU KNOW, "WE'VE SHOWN THIS OPERATION CODE IN A PREFERRED EMBODIMENT. THOSE OF ORDINARY SKILL IN THE ART WILL UNDERSTAND THAT AN OPERATION CODE CAN BE TRANSMITTED IN OTHER WAYS," FOR EXAMPLE.

OKAY. THAT KIND OF A DISCLOSURE IS NOT IN THIS SPECIFICATION.

I THINK THAT ANSWERS THE QUESTION.

THE COURT: YEAH.

MR. BROWN: MR. DETRE, AND RAMBUS, OVER QUITE A BIT OF TIME NOW, HAS SPENT -- HAS REPEATEDLY SAID THAT THERE ARE MULTIPLE INVENTIONS DISCLOSED IN THESE PATENTS, AND I'LL AGREE THAT THERE ARE MULTIPLE INVENTIONS DISCLOSED IN THESE PATENTS, OKAY.

BUT EVEN AGREEING TO THAT, AGREEING THAT THERE ARE MULTIPLE INVENTIONS DISCLOSED IN THESE PATENTS SAYS NOTHING ABOUT WHAT THOSE INVENTIONS ARE.

WHAT'S IMPORTANT IS WHAT IS IN THE CLAIMS.

BUT I DO WANT TO GO BACK AND TAKE ISSUE WITH A COUPLE OF THINGS THAT MR. DETRE HAS SAID, AND THAT IS THAT BACK IN THE ORIGINAL CLAIMS, THERE

WAS SOMETHING LIKE -- IN THE CLAIMS AS ORIGINALLY FILED, THERE WERE, I THINK, 25 DIFFERENT INDEPENDENT CLAIMS AND THERE WAS A RESTRICTION REQUIREMENT THAT WAS ISSUED.

THERE -- AND THERE WAS A RESTRICTION REQUIREMENT BASICALLY, WHICH IS THE PATENT OFFICE PROCEDURE BY WHICH BASICALLY THE EXAMINER SAYS "I ONLY WANT TO EXAMINE THIS SET OF CLAIMS IN THIS SET OF APPLICATIONS. IF YOU WANT ME TO EXAMINE THE NEXT SET OF CLAIMS, YOU HAVE TO FILE ANOTHER APPLICATION."

AND THERE WAS AN 11 WAY RESTRICTION REQUIREMENT. SORRY, THAT'S A PATENTESE THING.

OF THOSE 11 SETS OF CLAIMS THAT THE EXAMINER REQUIRED THEM TO DIVIDE OUT, NINE OF THOSE SETS OF CLAIMS, THAT IS, ALL BUT TWO OF THE INDEPENDENT CLAIMS THAT WERE IN THAT APPLICATION REQUIRED, RECITED SPECIFICALLY A BUS WHICH COMPRISED A SET OF SIGNAL LINES OVER WHICH SUBSTANTIALLY ALL ADDRESS DATA AND CONTROL NEEDED FOR COMMUNICATION WITH THE OTHER DEVICES IS TRANSMITTED, AND IN WHICH THE NUMBER OF BITS IN A SINGLE ADDRESS IS -- SORRY -- THE NUMBER OF BUS LINES IS SUBSTANTIALLY FEWER THAN THE NUMBER OF BITS IN A SINGLE ADDRESS.

THEY WERE -- I MEAN, ALL BUT TWO OF THE INDEPENDENT CLAIMS HAD BOTH OF THOSE LIMITATIONS IN THEM.

BUT NEVERTHELESS, THERE -- THOSE, THOSE REMAINING 23 CLAIMS WERE DIVIDED UP INTO NINE DIFFERENT INVENTIONS.

WHY WERE THEY DIVIDED UP INTO NINE DIFFERENT INVENTIONS?

IT'S BECAUSE THERE ARE OTHER FEATURES, SUCH AS AN ACCESS TIME REGISTER, SUCH AS A PACKET PROTOCOL, SUCH AS THE VARIABLE BLOCK SIZE INFORMATION, THAT CAN BE USED WITH THAT KIND OF A BUS, BUT DON'T NECESSARILY HAVE TO BE USED WITH THAT KIND OF A BUS.

SO THE DIFFERENT INVENTIONS WERE, BY AND LARGE, THIS PARTICULAR DEFINED BUS, OR THE BUS DEFINED BY THOSE TWO REQUIREMENTS, IN COMBINATION WITH SOME OF THESE SUBFEATURES, LIKE BLOCK SIZE, LIKE AN ACCESS TIME REGISTER, LIKE A PACKET, THAT COULD BE USED WITH THIS BUS, THAT COULD BE USED IN COMBINATION, THAT IS, YOU COULD HAVE TWO OF THESE SUBFEATURES WITH THAT ONE BUS.

BUT IN ALL CASES, THE DIFFERENT INVENTIONS WERE THIS, WHAT WE'VE BEEN CALLING, WHAT I'VE BEEN CALLING ANYWAY, A NARROW MULTIPLEXED BUS

IN COMBINATION WITH ONE OF THESE OTHER THINGS.

NOW, RAMBUS IS USING THIS NOW TO EXALT THE COMBINATION OF AN ACCESS TIME REGISTER WITH THE NARROW BUS, OR, SORRY, TO EXALT THE ACCESS TIME REGISTER ITSELF, RATHER THAN A SUBFEATURE THAT CAN BE USED WITH THE NARROW MULTIPLEXED BUS, THEY'RE EXALTING IT TO AN INVENTION ON ITS OWN.

THEY'RE DOING THE SAME THING WITH BLOCK SIZE INFORMATION, AND THEY'RE DOING THE SAME THING WITH AN OPERATION CODE.

THERE IS AN OPERATION CODE THAT'S MENTIONED IN ONE OR MORE OF THE CLAIMS OF THE ORIGINAL APPLICATION, AND I CAN'T HONESTLY TELL YOU WHICH ONE IT IS RIGHT NOW.

BUT BASICALLY IT TALKS ABOUT HAVING AN OPERATION CODE IN A PACKET ON THIS KIND OF A BUS THAT BASICALLY TRANSMITS A READ, OR TELLS THE DEVICE, OR TELLS THE MEMORY TO DO A READ OPERATION.

PARTICULARLY IN THE CONTEXT OF THE STATEMENTS IN THE SPECIFICATION THAT THE INVENTION IS A BUS ARCHITECTURE AND A SUBSYSTEM THAT INCLUDES THE FEATURE THAT ALL ADDRESS DATA IN CONTROL IS TRANSMITTED, OR SUBSTANTIALLY ALL ADDRESS DATA IN CONTROL IS SUBMITTED, IS TRANSMITTED OVER THE SET OF BUS LINES, AND THE BUS WHICH, WHERE THE NUMBER

OF BITS IN AN ADDRESS IS SUBSTANTIALLY GREATER THAN THE NUMBER OF LINES IN THE BUS, PARTICULARLY IN VIEW OF THAT LANGUAGE, THAT THAT IS THE INVENTION, OR THE CHARACTERIZATION OF THE INVENTION, ONE OF ORDINARY SKILL WOULD NOT READ THAT SPECIFICATION WHEN IT COMES DOWN TO THE PARTICULAR PACKET PROTOCOL AND THE MENTION, ONE MENTION, TWO MENTIONS ACTUALLY, OF AN OP CODE THAT ARE WITHIN THAT PACKET, ONE OF ORDINARY SKILL IN THE ART WOULD NOT TAKE THAT AS A DISCLOSURE THAT THE OP CODE CAN BE TAKEN OUT OF THE PACKET, CAN BE TAKEN OUT OF THE PACKET PROTOCOL, CAN BE TAKEN OUT OF THE BUS ARCHITECTURE AND SORT OF SET ASIDE AS A COMPLETELY SEPARATE INVENTION, WHICH IS WHAT RAMBUS IS TRYING TO DO NOW.

AND THE FACT IS THAT THERE IS NO DISCLOSURE IN THE SPECIFICATION AS FILED OF AN OPERATION CODE, EXCEPT IN THE CONTEXT OF A PACKET.

THE COURT: AND YOU WOULD DEFINE "PACKET" HOW?

MR. BROWN: IT'S, AGAIN, ONE OF THOSE THINGS THAT I CAN CERTAINLY GIVE YOU EXAMPLES OF A PACKET, AND YOU'VE PROBABLY LOOKED AT FIGURE 4 OF THIS PATENT MORE OFTEN THAN YOU WOULD CARE TO, SO I'M NOT GOING TO MAKE YOU LOOK AT IT AGAIN.

BUT A PACKET IS A SET OF RELATED INFORMATION, OKAY, THAT IS AT LEAST LOGICALLY RELATED; THAT IS, THAT IT'S A SET OF INFORMATION THAT GOES TOGETHER, OKAY, THAT IS TRANSMITTED IN SOME KIND OF A SEQUENCE OVER THE BUS.

THE COURT: OKAY.

MR. BROWN: OKAY?

THE COURT: YES.

ALL RIGHT. LET'S TAKE A BREAK.

MR. BROWN: OKAY.

THE COURT: WHY DON'T WE TRY AND BE BACK AT TEN OF 4:00.

(WHEREUPON, A RECESS WAS TAKEN.)

THE COURT: I DON'T WANT TO GET SIDE TRACKED, BUT LET ME JUST READ, AND THIS IS ACTUALLY FROM THE NORTHERN DISTRICT MODEL INSTRUCTIONS, AN INSTRUCTION ON WRITTEN DESCRIPTION.

IT READS, IN PART, "THE WRITTEN DESCRIPTION REQUIREMENT IS SATISFIED IF PERSONS OF ORDINARY SKILL IN THE FIELD WOULD RECOGNIZE FROM THE PATENT APPLICATION AS FIRST FILED THAT THE INVENTOR HAD IN MIND AT THAT TIME THE FULL SCOPE OF THE INVENTION AS FINALLY CLAIMED IN THE PATENT.

A REQUIREMENT IN A CLAIM NEED NOT BE SPECIFICALLY DISCLOSED IN THE ORIGINAL PATENT

APPLICATION IF PERSONS OF ORDINARY SKILL IN THE FIELD, READING THAT APPLICATION, WOULD UNDERSTAND THAT THE MISSING REQUIREMENT MUST NECESSARILY BE PRESENT."

DO EITHER OF YOU QUARREL WITH THAT AS AN ACCURATE STATEMENT OF THE LAW?

MR. DETRE: I DON'T, YOUR HONOR.

MR. BROWN: NO.

THE COURT: SO DOESN'T THIS QUESTION AS TO COMMUNICATION OTHER THAN IN A PACKET WOULD BE RECOGNIZED AS SOMETHING THAT MUST NECESSARILY BE PRESENT IN THE INVENTION AS DISCLOSED?

MR. BROWN: THAT IS CORRECT, YOUR HONOR.

MR. DETRE: COULD I ADDRESS THAT, AND MAYBE ALSO SOME OF THE OTHER POINTS MR. BROWN MADE?

THE COURT: BUT DO YOU AGREE THAT THAT'S THE QUESTION?

MR. DETRE: I AGREE THAT THAT'S THE QUESTION.

BUT WITH RESPECT TO DISTINCT INVENTIONS IN THIS CASE, SO WE HAVE TO LOOK AT THE INVENTIONS SEPARATELY AND UNDERSTAND, WITH RESPECT TO THE DISTINCT INVENTIONS, WHETHER A PERSON OF ORDINARY SKILL WOULD UNDERSTAND THAT, WITH RESPECT TO THAT DISTINCT INVENTION, SOME FORM OF OPERATION CODE

MUST NECESSARILY BE SENT, AND IT NEED NOT BE RESTRICTED TO THE KIND OF OPERATION CODE IN ONE OF THE OTHER DISTINCT INVENTIONS.

THE COURT: OKAY. I THINK I UNDERSTAND BOTH YOUR ARGUMENTS ON THAT, BUT LET ME ASK, BEFORE I LET YOU GO FURTHER, WHAT OF THE REST OF THE MOTIONS ARE YOU PARTICULARLY ANXIOUS TO ADDRESS?

MR. BROWN: I THINK WE'RE PARTICULARLY, ON THE -- WE SHOULD TALK ABOUT THE FIRST AND SECOND EXTERNAL CLOCK ISSUE.

THE COURT: OKAY. YEAH, THAT'S ONE I'M INTERESTED IN.

WHAT ARE YOU PARTICULARLY INTERESTED IN ADDRESSING?

MR. DETRE: IF YOUR HONOR DOESN'T HAVE ANY PARTICULAR CONCERNS ABOUT OTHER ISSUES, I DON'T THINK WE NEED TO ADDRESS ANY OF THEM AND WE'LL STAND ON OUR PAPERS.

THE COURT: OKAY. DO YOU WANT TO --

MR. DETRE: I MIGHT SAY ACTUALLY, I'LL TAKE THAT BACK, MAYBE ON SYNCHRONOUS MEMORY DEVICE I HAVE A FEW THINGS TO SAY.

THE COURT: OKAY. WHY DON'T YOU GO AHEAD AND MAKE THE ADDITIONAL COMMENTS YOU WANTED TO ON THE ISSUE THAT YOU STARTED TO TALK ABOUT,

RECOGNIZING THAT I THINK I UNDERSTAND IT, AND THEN WE'LL GO TO THE CLOCKS AND WE'LL END WITH THE SYNCHRONOUS MEMORY DEVICE.

MR. DETRE: THANK YOU, YOUR HONOR.

I MAY HAVE SAID THIS BEFORE, BUT I JUST WANTED TO POSSIBLY REITERATE ONE POINT IN RESPONSE TO SOMETHING MR. BROWN SAID ABOUT ACCESS MODES AND ACCESS TYPES, AND THAT IS THAT THE PATENT SPECIFICATION IS QUITE CLEAR THAT THE ACCESS MODE IS DETERMINED BY THE ACCESS TYPE FIELD, AND THAT ACCESS TYPE FIELD IS FOUR BITS, WHICH IN THE PREFERRED EMBODIMENT ARE ALL RECEIVED IN PARALLEL, AND THAT'S WHAT THE FEDERAL CIRCUIT FOUND FOR AN EMBODIMENT TO CORRESPOND TO A READ REQUEST.

THE SECOND POINT --

THE COURT: WHAT LANGUAGE DO YOU THINK SUPPORTS THAT LAST STATEMENT?

MR. DETRE: OH, IN THE SPECIFICATION THAT THE --

THE COURT: NO, THAT THE FEDERAL CIRCUIT FOUND THAT TO BE A READ REQUEST?

MR. DETRE: OH. LET ME GO TO THE FEDERAL CIRCUIT OPINION.

THE FEDERAL CIRCUIT, AT THE BEGINNING -- AT THE TOP OF PAGE 1092 IN THE OPINION, AFTER

COMPARING THE PARTIES' RESPECTIVE POSITIONS, THE FEDERAL -- LET ME START THERE, ACTUALLY, ON PAGE 1091. THE FEDERAL CIRCUIT IS COMPARING THE PARTIES' RESPECTIVE POSITIONS AND NOTES THAT INFINEON ARGUED THAT THE READ REQUEST MUST CONTAIN ALL INFORMATION NECESSARY TO PERFORM THE REQUESTED READ, AND THEN NOTED THAT RAMBUS'S POSITION, TO THE CONTRARY, WAS THAT THE READ REQUEST IN THE PREFERRED EMBODIMENT IS, QUOTE, "ONE COMPONENT OF THE REQUEST PACKET COMPRISING THE FIRST FOUR BITS OF THE PACKET."

AND THEN THE FEDERAL CIRCUIT HAS THE FIGURE 4 SHOWING --

PERHAPS WE CAN PULL THAT UP, FROM ANY OF THE PATENTS, FIGURE 4. MOVE FORWARD A FEW PAGES. THERE WE GO AT THE BOTTOM, FIGURE 4.

THE FEDERAL CIRCUIT REPRODUCED FIGURE 4 AND TALKED ABOUT, "AS SHOWN ABOVE, THE REQUEST PACKET HAS MULTIPLE FIELDS, INCLUDING AN ACCESS TYPE FIELD," AND THAT'S THE FIRST FOUR BITS ALL IN THE TOP LINE OF THE PACKET, ONLY PART OF THE TOP LINE OF THE PACKET.

AND THEN THE FEDERAL CIRCUIT PROCEEDS TO ANALYZE WHETHER A READ REQUEST MUST CONTAIN MORE INFORMATION THAN WHAT'S CONTAINED IN THE ACCESS

TYPE FIELD.

AND IT CONCLUDES NEAR THE TOP OF PAGE 1093. "CONTRARY TO INFINEON'S POSITION, IN ACCORD WITH RAMBUS'S POSITION, THAT REFERENCES IN THE SPECIFICATION TO READ REQUESTS DO NOT SUGGEST THE PRESENCE OF ADDRESS AND CONTROL INFORMATION.

THE SPECIFICATION MERELY INDICATES THAT THE READ REQUEST REQUESTS DATA FROM A MEMORY DEVICE AND SPECIFIES WHAT TYPE OF READ (E.G., PAGE MODE, NORMAL MODE, ET CETERA) TO PERFORM."

"MOREOVER," THE FEDERAL CIRCUIT GOES ON, "THE DEPENDENT CLAIMS DEMONSTRATE THAT READ REQUEST IS DISTINCT FROM A REQUEST PACKET."

SO THE FEDERAL CIRCUIT WAS CONSIDERING INFINEON'S POSITION THAT THE READ REQUEST HAD TO BE THE WHOLE REQUEST PACKET, RAMBUS'S POSITION THAT THE READ REQUEST HAD TO BE JUST THAT ACCESS TYPE, ZERO TO THREE, AND SIDED WITH RAMBUS THAT ALL OF THIS OTHER INFORMATION, ADDRESS INFORMATION AND CONTROL INFORMATION LIKE THE BLOCK SIZE -- AND THAT'S ALL THERE IS ONCE YOU GET PAST THIS FIRST LINE, ALL YOU'VE GOT IS ADDRESS INFORMATION AND SOME CONTROL INFORMATION -- AND THE FEDERAL CIRCUIT FOUND THAT THAT DID NOT NEED TO BE IN THE READ REQUEST.

SO WHAT THE FEDERAL CIRCUIT WOUND UP WITH, FOR PURPOSES OF THE PREFERRED EMBODIMENT, WAS TO AGREE WITH RAMBUS THAT, IN THE PREFERRED EMBODIMENT, ONLY THE ACCESS TYPE WHICH REQUESTS, WHICH SPECIFIES THAT IT'S A READ AND IDENTIFIES THE TYPE OF READ, IS THE READ REQUEST.

AND THAT'S WHAT IT WAS LOOKING AT WHEN IT CAME UP WITH ITS CONSTRUCTION WHICH, WHICH SAID A SERIES OF BITS.

SO THERE ARE THE SERIES. THEY'RE A SERIES IN THE PREFERRED EMBODIMENT IN SPACE, A SPACIAL SERIES, ONE NEXT TO THE OTHER, NOT IN TIME ONE AFTER THE OTHER.

THE COURT: OKAY.

MR. DETRE: THE SECOND POINT I WANTED TO MAKE, YOUR HONOR, AND I THINK, YOU KNOW, AS THE MODEL INSTRUCTION YOU READ INDICATES, THIS ALL COMES DOWN TO THE UNDERSTANDING OF A PERSON OF ORDINARY SKILL.

AND CERTAINLY IT'S A FACTUAL ISSUE, BUT IT'S CLEAR TO US THAT AT A VERY MINIMUM THERE'S A MATERIAL DISPUTE OF FACT.

AND LET ME STRESS ALSO THAT HYNIX, ON THE VALIDITY ISSUES, HAS THE BURDEN OF PROVING INVALIDITY BY CLEAR AND CONVINCING EVIDENCE, AND

THAT, OF COURSE, ALSO IS THE STANDARD TO BE CONSIDERED ON SUMMARY JUDGMENT.

THE COURT: BUT LET ME STOP YOU FOR A MINUTE, BECAUSE I THINK THIS IS A DISTINCTION, AT LEAST, THAT I'VE ALWAYS THOUGHT EXISTED -- AND I MAY BE WRONG -- BUT IF YOU'RE TALKING ABOUT SOMETHING LIKE OBVIOUSNESS, YOU'RE TALKING ABOUT WHAT WOULD BE OBVIOUS TO SOMEONE SKILLED IN THE ART FROM READING THIS DISCLOSURE.

IN THE WRITTEN DESCRIPTION REQUIREMENT, YOU'RE TRYING TO DETERMINE WHETHER OR NOT THE INVENTOR HAD THAT INVENTION IN MIND AT THE TIME, AND IF IT'S NOT EXPRESSLY SET FORTH, YOU'VE GOT TO SAY THAT SOMEONE READING IT WOULD UNDERSTAND THAT WHATEVER WAS MISSING MUST NECESSARILY BE PRESENT.

IN OTHER WORDS, YOU COULDN'T HAVE THE INVENTION WITHOUT IT.

MR. DETRE: YES, FROM THE UNDERSTANDING OF A PERSON OF ORDINARY SKILL IN THE ART, AND THE CASES ARE CLEAR THAT THAT'S A FACTUAL ISSUE. IT'S A FACT QUESTION.

THE COURT: WELL, NORMALLY IT IS.

MR. DETRE: YES.

THE COURT: ALL RIGHT.

MR. DETRE: AND WHAT I WOULD -- AND I

THINK IT'S PRETTY CLEAR, AND IT'S OUR POSITION CERTAINLY THAT IT'S PRETTY CLEAR, THAT A PERSON OF ORDINARY SKILL IN THE ART HERE WOULD UNDERSTAND THAT THERE ARE DISTINCT INVENTIONS, AND WHEN THAT PERSON OF ORDINARY SKILL IS LOOKING AT ONE OF THE INVENTIONS THAT IS NOT RELATED TO THE PACKET, THE PERSON OF ORDINARY SKILL WOULD UNDERSTAND THAT TO UTILIZE THAT INVENTION, YOU NEEDED TO HAVE A READ REQUEST OR AN OPERATION CODE SPECIFYING A READ OPERATION SENT IN SOME FORM. FOR EXAMPLE, FOR THE ACCESS TIME REGISTER, IT WOULDN'T HAVE TO BE IN THE WAY THAT ANOTHER DISTINCT INVENTION SPECIFIED.

AND IT CAN'T BE THAT THE UNDERSTANDING OF A PERSON OF ORDINARY SKILL IN THE ART WOULD TURN ON WHETHER SOME, YOU KNOW, ESSENTIALLY BOILER PLATE WAS INCLUDED. "AND BY THE WAY, TO USE AN ACCESS TIME REGISTER, YOU DON'T HAVE TO SEND AN OPERATION CODE IN A PACKET."

I THINK A PERSON OF ORDINARY SKILL'S UNDERSTANDING GOES BEYOND THAT AND UNDERSTANDS HOW TO USE DIFFERENT INVENTIONS IN DIFFERENT WAYS.

YOU KNOW, THE PATENT SPECIFICATION SHOWS A PARTICULAR KIND OF OUTPUT DRIVER, FOR EXAMPLE.

BUT NOBODY WOULD THINK THAT IN ORDER TO USE A PARTICULAR CLOCKING SCHEME DISCLOSED IN THE

PATENT OR IN ORDER TO USE AN ACCESS TIME REGISTER OR IN ORDER TO USE THE BLOCK SIZE INFORMATION INVENTION, THAT YOU COULD ONLY USE THOSE WITH THIS PARTICULAR KIND OF OUTPUT DRIVER. THAT'S, THAT'S THE ISSUE AND I THINK IT'S PRETTY CLEAR.

I DID WANT TO POINT YOU TO A COUPLE OF THE ORIGINAL CLAIMS. I MENTIONED IN MY ARGUMENT THAT SOME ORIGINAL CLAIMS REFERRED TO A PACKET AND SOME DID NOT.

THIS IS -- I WON'T BELABOR THE POINT TOO MUCH. I'LL JUST DIRECT YOUR HONOR TO THE ORIGINAL APPLICATION THAT IS ATTACHED TO MR. BROWN'S DECLARATION IN SUPPORT OF HYNIX'S SUMMARY JUDGMENT MOTIONS. IT'S EXHIBIT 76.

AND AT PAGE 103, INTERNAL PAGE NUMBER 103 OF THE APPLICATION, WHICH BY HAPPY COINCIDENCE IS ALSO CLAIM 103, WHICH TALKS ABOUT -- IT'S A LENGTHY CLAIM, BUT IN PARTICULAR AT THE END IT TALKS ABOUT RESPONDING TO A REQUEST WHILE, JUST AS ANOTHER EXAMPLE, THERE ARE OTHERS, BUT JUST AS ANOTHER EXAMPLE, CLAIM 24, CLAIM 124, EXCUSE ME, WHICH IS ON PAGE 112 TO 113, TALKS ABOUT RESPONDING TO A REQUEST PACKET.

SO THERE IS A DISCLOSURE IN THE ORIGINAL APPLICATION IN ONE CLAIM OF A REQUEST, IN THE OTHER

CLAIM OF A REQUEST PACKET, AND I THINK A PERSON OF ORDINARY SKILL IN THE ART WOULD UNDERSTAND THAT THE FORMER IS BROADER THAN THE LATTER.

I WOULD ALSO NOTE THAT THERE ARE -- MR. BROWN, IN HIS ARGUMENT, SUGGESTED THAT THE WRITTEN DISCLOSURE REALLY HAD TO DISCLOSE EXACTLY WHAT YOU'RE CLAIMING, AND THAT IS SIMPLY NOT THE CASE.

AND THERE ARE -- WE CITE VARIOUS CASES --

THE COURT: YEAH, I'M PRETTY FAMILIAR WITH THAT.

MR. DETRE: OKAY.

THE COURT: "IT IS NOT A QUESTION WHETHER ONE SKILLED IN THE ART MIGHT BE ABLE TO CONSTRUCT THE PATENTEE'S DEVICE FROM THE TEACHINGS OF THE DISCLOSURE OF THE APPLICATION. RATHER, IT IS A QUESTION OF WHETHER THE APPLICATION NECESSARILY DISCLOSES THAT PARTICULAR DEVICE."

MR. DETRE: OKAY. BUT THERE ARE VARIOUS CASES, AND WE CITE MANY OF THEM IN OUR PAPERS, WHERE THERE'S A CERTAIN DISCLOSURE IN THE PATENT APPLICATION AND BROADER CLAIMS ARE HELD TO BE SUPPORTED BECAUSE OF THE UNDERSTANDING OF A PERSON OF ORDINARY SKILL IN THE ART.

ONE EXAMPLE IS THE LAMPI CORP. VERSUS

AMERICAN POWER PRODUCTS CASE, 228 F.3D 1365. THE WRITTEN DESCRIPTION ONLY TALKED -- THIS WAS FOR A CERTAIN KIND OF FLORESCENT LIGHT AND THERE WERE TWO HALF SHELLS USED TO CONSTRUCT IT, AND THE WRITTEN DESCRIPTION ONLY TALKED ABOUT IDENTICAL HALF SHELLS, AND THEN, IN FACT, MENTIONED THE ADVANTAGES OF HAVING IDENTICAL HALF SHELLS.

AND NEVERTHELESS, THE FEDERAL CIRCUIT HELD THAT CLAIMS THAT HAVE SHELLS THAT WERE NOT IDENTICAL WERE SUPPORTED BY THE WRITTEN DESCRIPTION. A PERSON OF ORDINARY SKILL IN THE ART WOULD UNDERSTAND THAT WHILE YOU MAY WANT IDENTICAL HALF SHELLS FOR CERTAIN REASONS, YOU COULD USE HALF SHELLS THAT WERE NOT IDENTICAL.

CORDIS CORP. VERSUS MEDTRONIC, 339 F.3D 1352, IN THAT CASE THE PATENT WAS ABOUT A KIND OF A STINT USED IN BALLOON ANGIOPLASTY, AND ALL THAT WAS SHOWN IN THE WRITTEN DESCRIPTION WERE ALTERNATING COMPLETE AND HALF SLOTS AT THE END, AND THE FEDERAL CIRCUIT HELD THAT CLAIMS THAT DID NOT RESTRICT, THAT WERE NOT RESTRICTED IN THAT WAY WERE SUPPORTED BY THE WRITTEN DESCRIPTION.

THE COURT: OKAY.

MR. DETRE: AND THOSE ARE CASES THAT DO NOT RAISE THE SORT OF DISTINCT INVENTION ISSUE THAT

I MENTIONED BEFORE.

BUT EVEN IN THOSE CASES, YOU WEREN'T RESTRICTED TO EXACTLY WHAT WAS IN THE WRITTEN DESCRIPTION.

THE LAST THING I WANT TO MENTION IN RESPONSE TO WHAT MR. BROWN SAID, MR. BROWN FOCUSSED ON THE ORIGINAL RESTRICTION REQUIREMENT AND SUGGESTED THAT THAT SOMEHOW SHOWED THAT ALL OF THE CLAIMS WERE JUST SORT OF SHOWING THESE FEATURES, LIKE THE ACCESS TIME REGISTER, THAT COULD BE USED WITH THE PARTICULAR BUS ARCHITECTURE.

AND I WOULD LIKE TO JUST NOTE ANOTHER PART OF THE FEDERAL CIRCUIT OPINION WHERE THEY DISCUSS A LATER RESTRICTION REQUIREMENT, AND I'LL JUST QUOTE FROM THE OPINION.

THE FEDERAL -- THIS IS AT PAGE 1095 OF THE FEDERAL CIRCUIT OPINION AFTER DISCUSSING THE ORIGINAL RESTRICTION REQUIREMENT. THE FEDERAL CIRCUIT NOTES, "LATER, DURING PROSECUTION OF THE '580 PATENT," WHICH IT NOTES IS THE GRANDPARENT OF THE '918 PATENT AND THE PARENT OF THE '263 PATENT, "THE PTO ISSUED A TWO-WAY RESTRICTION DIVIDING THE CLAIMS INTO TWO DISTINCT GROUPS, A MULTIPLEXING BUS GROUP, GROUP I, AND A LATENCY INVENTION GROUP, GROUP II. THIS TWO-WAY RESTRICTION STATED, 'THE

MEMORY DEVICE IN GROUP I DOES NOT REQUIRE THE ACCESS TIME REGISTER OF GROUP II. AND THE SEMICONDUCTOR DEVICE IN GROUP II DOES NOT REQUIRE THE PLURALITY OF CONDUCTOR BEING MULTIPLEXED TO RECEIVE AN ADDRESS AS CLAIMED IN GROUP I.'"

AND THEN THE FEDERAL CIRCUIT GOES ON, "RAMBUS ELECTED TO PROSECUTE THE LATENCY, NAMELY, PROCESS TIME REGISTER, IN THE '580 PATENT, THEREFORE THE CLAIMS OF THE '580 PATENT DO NOT REQUIRE A MULTIPLEXING BUS."

SO IT'S PRETTY CLEAR IN THE PTO'S VIEW, AND IN THE FEDERAL CIRCUIT'S VIEW, THAT VARIOUS RAMBUS INVENTIONS, INCLUDING, FOR EXAMPLE, THE ACCESS TIME REGISTER INVENTION AT ISSUE HERE, IS A SEPARATE INVENTION FROM THE BUS.

THE COURT: OKAY. YOU WANT TO TALK ABOUT THE CLOCKS?

MR. BROWN: I JUST HAVE A COUPLE OF COMMENTS IN RESPONSE TO MR. DETRE.

THE COURT: OKAY.

MR. BROWN: THERE'S BEEN A LOT OF BACK AND FORTH ABOUT, YOU KNOW, JUST, YOU KNOW, THE INDIVIDUAL PARSING OF WORDS AND PHRASES AND TRYING TO DIVINE INTENT FROM THE FEDERAL CIRCUIT OPINION, AND I CONTINUE TO DISAGREE WITH SOME OF WHAT

MR. DETRE SAID, BUT IF IT WOULD BE HELPFUL TO THE COURT, WE COULD SUBMIT SOME ADDITIONAL BRIEFS OR A SHORT BRIEF ON THIS ISSUE ON, YOU KNOW, I -- I JUST DON'T THINK THAT, YOU KNOW, TRYING TO -- THAT SPECULATING ABOUT WHAT ET CETERA MEANS, OR WHAT E.G. MEANS IS A BASIS TO, YOU KNOW -- WOULD BE A FIRM BASIS ON WHICH TO GRANT RAMBUS'S MOTION ON THIS POINT OF READ REQUEST.

THE COURT: OKAY.

MR. BROWN: OKAY.

THE COURT: YOU WANT TO GO TO CLOCKS?

MR. BROWN: YES. ACTUALLY, MR. JONES IS GOING TO DO THAT, BUT I HAVE TO SET HIM UP HERE.

THE COURT: OKAY.

MR. BROWN: I THINK THIS IS IT.

MR. JONES: YES.

YOUR HONOR, IN LIGHT OF THE TENTATIVE RULING YESTERDAY WITH RESPECT TO THE CONSTRUCTION OF SECOND EXTERNAL CLOCK, I'M REALLY GOING TO FOCUS ON HYNIX'S MOTION FOR NONINFRINGEMENT UNDER HYNIX'S PROPOSED CONSTRUCTION, WHICH IS CONSISTENT, IF NOT IDENTICAL, WITH THE TENTATIVE FROM YESTERDAY.

THE "SECOND EXTERNAL CLOCK" TERM IS RECITED IN VARIOUS PATENTS, INCLUDING THE '214, THE '105, THE '365 AND THE '152 PATENTS. THE '214

PATENT IS LISTED FIRST AND IS ALSO MENTIONED IN THE PAPERS IN TERMS OF THE, THE PATENT IN WHICH INFINEON WAS GRANTED -- OR THE COURT FOUND FOR INFINEON IN FAVOR OF NONINFRINGEMENT DUE TO A FAILURE OF PROOF ON THE PART OF RAMBUS IN THAT LITIGATION.

HOWEVER, MOVING ON TO THE MERITS IN TERMS OF THE CONSTRUCTION PROPOSED BY HYNIX AND THE COURT'S TENTATIVE CONSTRUCTION, THE ONLY ISSUE HERE, AND I'LL MOVE TO THE CONSTRUCTION PROPOSED BY HYNIX, AND THAT WAS, OR IS, "A PERIODIC SIGNAL RECEIVED BY THE MEMORY DEVICE FROM AN EXTERNAL SOURCE TO PROVIDE SECOND TIMING INFORMATION THAT IS DIFFERENT FROM THE FIRST TIMING INFORMATION."

IN THIS INSTANCE, THE FIRST TIMING INFORMATION IS PROVIDING REFERENCE TO THE FIRST EXTERNAL CLOCK, AND THE PURPOSE OF THE DEFINITION AS RECITED, EXPLICITLY RECITED, IS THAT THE TWO CLOCKS, THE TWO EXTERNAL CLOCKS ARE PROVIDING DIFFERENT TIMING INFORMATION.

NOW, IN TERMS OF THE INFRINGEMENT ALLEGATIONS AGAINST THE ACCUSED HYNIX DOUBLE DATA RATE SDRAM PRODUCTS, DRAM PRODUCTS, RAMBUS IS ESSENTIALLY CONTENDING THAT THE USE OF COMPLEMENTARY CLOCKS THAT ARE FED INTO THE DEVICES

EXTERNALLY, AND THAT'S IDENTIFIED HERE AS CK AND CK BAR, ARE ESSENTIALLY TWO EXTERNAL CLOCKS.

NOW, UNDER THE DEFINITION THAT'S PROFFERED BY HYNIX AND WHICH WAS REFLECTED IN THE COURT'S TENTATIVE AS OF YESTERDAY, WHAT CAN BE SEEN HERE FROM THIS DIAGRAM IS THE USE OF CLOCK AND CLOCK BAR, IN THIS SENSE THEY ARE COMPLEMENTARY CLOCKS, AND I'LL JUST READ HERE FROM A DATA SHEET OF AN ACCUSED HYNIX DEVICE.

AND UP HERE IN THE DESCRIPTION IT SAYS, IT SAYS THAT "CLOCK AND CLOCK BAR ARE DIFFERENTIAL CLOCK INPUTS. ALL ADDRESS AND CONTROL INPUT SIGNALS ARE SAMPLED ON THE CROSSING AND POSITIVE EDGE OF CLOCK AND NEGATIVE EDGE OF CLOCK BAR. OUTPUT," AND THEN PARENTHETICALLY, "(READ DATA IS REFERENCED TO THE CROSSINGS OF CLOCK AND CLOCK BAR)" PARENTHETICALLY, "BOTH DIRECTIONS OF CROSSING."

WHAT'S IDENTIFIED HERE WITH THE THREE ARROWS IS REFLECTIVE OF WHAT THAT DESCRIPTION DESCRIBES.

THE TIMING INFORMATION PROVIDED BY CLOCK AND CLOCK BAR ARE ESSENTIALLY IDENTICAL. THE DEVICES THAT ARE, THAT ARE RECEIVING THESE CLOCK INPUTS ARE USING THE INFORMATION THAT'S PROVIDED AT

THE CROSSING POINTS OF CLOCK AND CLOCK BAR, NOT IN CONTRAST TO WHAT'S DISCLOSED IN THE PREFERRED EMBODIMENT AND THE CLOCKING SCHEME OF THE RAMBUS PATENTS, NOT THE CLOCK EDGES OF ONE VERSUS THE CLOCK EDGES OF ANOTHER TAKEN AT A DIFFERENT TIME, BUT INSTEAD HERE, IDENTICAL TIMING INFORMATION.

AND THE QUESTION COULD BE PHRASED LIKE THIS: AT ANY GIVEN TIME, ARE THE CLOCKS PROVIDING DIFFERENT TIMING INFORMATION TO THE DEVICE?

AND THE ANSWER TO THAT QUESTION IS NO, AS CAN BE SEEN HERE.

WHAT'S HAPPENING IS IT'S -- THE CROSSING POINTS ARE WHERE THE TIMING INFORMATION IS BEING PROVIDED, NOT AT THE RISING EDGE OF ONE THAT'S NOT COINCIDENT WITH THE FALLING EDGE OF ANOTHER CLOCK IN THIS INSTANCE.

ONE OF THE ARGUMENTS, OR TWO OF THE ARGUMENTS THAT RAMBUS HAS MADE IS, FIRST, THAT EITHER THE DEVICES WOULD NOT OPERATE WITH JUST ONE OF THESE CLOCKS, OR THE DEVICES WOULD NOT OPERATE AS WELL.

AND THE POINT HERE ISN'T THAT, ISN'T THE QUESTION OF WHAT THE PURPOSE OF THE CLOCKS ARE.

YES, THE DEVICES OPERATE BETTER WITH COMPLEMENTARY CLOCKS AS OPPOSED TO A SINGLE CLOCK.

THE QUESTION IS, DO THE CLOCKS PROVIDE DIFFERENT TIMING INFORMATION?

AND FROM THE DEVICE'S PERSPECTIVE, THEY DO NOT, BECAUSE THE DEVICE IS ALWAYS TAKING THE INFORMATION FROM THE CROSSING POINT OF THE RISING EDGE OF ONE CLOCK AND THE FALLING EDGE OF ANOTHER.

THE SECOND ARGUMENT THAT RAMBUS MAKES IS THAT, OKAY, THE TIMING DIAGRAMS AND THE CLOCK SIGNALS, THEY'RE REALLY IDEALIZED. THEY'RE NEVER REALLY THIS PERFECT.

AND WHAT I'VE DONE HERE IN THIS SLIDE IS JUST KIND OF DEMONSTRATED, OR KIND OF ILLUSTRATED WHAT RAMBUS'S ARGUMENTS ARE.

THEIR ARGUMENT ESSENTIALLY BOILS DOWN TO SINCE THESE ARE NOT IDEALIZED, AT CERTAIN POINTS WHERE THAT CROSSING POINT TAKES PLACE, BECAUSE OF THE VARIATIONS IN THE RISE AND FALL TIMES OF THE CLOCKS NOT BEING EXACTLY WHAT'S SHOWN IN THE TIMING DIAGRAMS, YOU KNOW, THERE'S GOING TO BE SOME VARIATION AS TO WHERE THE TWO CLOCK EDGES INTERSECT AND CROSS.

THAT DOES NOT REALLY CHANGE THE ISSUE, OR TRANSFORM THE ISSUE IN ANY WAY.

WHAT'S STILL HAPPENING IS THAT THE TIMING INFORMATION, REGARDLESS OF WHETHER THERE'S SOME

VARIATION FROM THE IDEAL SITUATION, WHICH IS SHOWN IN THE FIRST CROSSING POINT ON THE LEFT, VERSUS THE NON-IDEAL CROSSING POINT, WHICH IS SHOWN AT A LOWER SECTION ON THE, IN THE MIDDLE AND THEN EVEN A HIGHER SECTION ON THE RIGHT, THE FACT REMAINS THE SAME, THAT IT IS THE CROSSING POINTS BETWEEN THOSE TWO SIGNALS WHICH IS PROVIDING THE TIMING INFORMATION. THEY ARE NOT PROVIDING DIFFERENT TIMING INFORMATION.

THE CLOCK AND CLOCK BAR ARE ESSENTIALLY MIRROR IMAGES, OR INVERSE IMAGES OF ONE ANOTHER, AND I THINK IT'S HELPFUL TO ACTUALLY LOOK AT THE CLOCKING SCHEME AT LEAST TO GIVE CONTEXT TO THIS, LOOK AT THE CLOCKING SCHEME THAT'S DISCLOSED IN THE PREFERRED EMBODIMENT OF THE RAMBUS PATENT.

FIGURE 8 OF THE PATENTS, AGAIN, THIS WAS ADDRESSED YESTERDAY AND I THINK EVEN IN THE TUTORIAL ON THURSDAY, SHOWS THE ONE AND ONLY CLOCKING SCHEME DISCLOSED IN THE PATENTS, AND THAT'S SHOWING CLOCK LINE 53, LOOPING CLOCK 1 OUT FROM THE CLOCK GENERATOR, AND THEN ONCE THAT CLOCK RETURNS ALONG THE U, IT'S FED AGAIN INTO THE TWO CHIPS THAT ARE CONNECTED, OR TWO DEVICES THAT ARE CONNECTED TO THE CLOCK BUS LINE.

NOW, WHAT'S INTERESTING ABOUT THAT IS IN

CONTRAST TO COMPLEMENTARY CLOCKS, THE ORDER IN WHICH THOSE CLOCKS ARE RECEIVED AT THOSE TWO DEVICES IS PROVIDING DIFFERENT TIMING INFORMATION.

FOR EXAMPLE, THE FIRST CHIP IN THIS INSTANCE, IT'S GOING TO BE CHIP 0, WILL RECEIVE CLOCK NUMBER 1 PRIOR TO CHIP N RECEIVING ANY INFORMATION, AND THAT'S PROVIDING A FIRST TIMING INFORMATION.

THEN THE NEXT THING THAT HAPPENS, AT LEAST IN FIGURE 8A THAT WAS SHOWN BEFORE, IS THAT IN SEQUENCE OF TIME, THE FIRST CLOCK EDGE IS NOW GOING TO REACH THE SECOND CHIP BECAUSE IT'S ON THE -- WHAT'S HAPPENING HERE IS THE FIRST CLOCK, CLOCK 1, IS GOING TO BE SAMPLED AND PROVIDE A TIMING INFORMATION TO CHIP 0.

THAT CLOCK PULSE IS GOING TO CONTINUE ALONG THE CLOCK BUS LINE 53 AND THEN BE RECEIVED AT CHIP N.

NOW, CLOCK 2 IS THE SAME SIGNAL ONCE IT'S TURNED AROUND AT THE U POINT.

NOW, RETURNING BACK TO THE DIAGRAM I WAS SHOWING, CLOCK 1 GETS RECEIVED AT CHIP O, THEN IT GETS RECEIVED AT CHIP N.

NOW, ONCE THE CLOCK SIGNAL HAS MADE ITS WAY AROUND THE U, IT'S GOING TO BE SAMPLED THIS

TIME AT CHIP N, AND IN THIS INSTANCE IT'S CALLED CLOCK 2, OR THE LATE CLOCK.

THEN FINALLY AS IT MAKES ITS WAY AROUND THE U, IT'S GOING TO BE RECEIVED AT CHIP O, WHICH WAS THE CHIP THAT WAS CLOSEST TO THE CLOCK GENERATOR IN THE PRIOR EXAMPLE.

NOW, WHAT CAN BE SEEN HERE IS THAT BOTH OF THESE CHIPS ARE RECEIVING TWO EXTERNAL CLOCKS, CLOCK 1 AND CLOCK 2, AND THEY'RE SAMPLING BOTH CLOCK 1, THE RISING EDGES OF BOTH CLOCK 1 AND CLOCK 2.

THEY'RE DOING THIS IN ORDER TO CORRECT FOR SKEW SO THAT THE, OR CLOCK SKEW SO THAT THE DEVICES THAT ARE ATTACHED TO THE BUS, NO MATTER WHERE THEY ARE, WILL BE ABLE TO OPERATE IN SYNC WITH ONE ANOTHER.

AND THE WAY THAT'S DONE IS IF YOU LOOK AT THE DOTTED LINE EXTENDING VERTICALLY ABOVE 59, ESSENTIALLY THE CLOCKING SCHEME TAKES THE TWO TIMING INFORMATIONS PROVIDED BY CLOCK 1 AND CLOCK 2 AND IT DERIVES THE MID-POINT, AND THAT MID-POINT, AS REFLECTED IN THIS DIAGRAM, THE MID-POINT FOR EACH OF THE DEVICES IS GOING TO BE THE SAME SO THAT OFF OF THAT MID-POINT FROM THOSE TWO CLOCKS, AN INTERNAL CLOCK CAN BE DERIVED.

BUT THE IMPORTANT THING IN NOTING THIS, AND THIS IS WHY THE DEFINITION THAT'S BEEN PROFFERED BY HYNIX IS THE ONE WHICH WE THINK IS CORRECT, IS THAT THE INFORMATION THAT'S BEING RECEIVED FROM EACH OF THOSE CLOCKS IS DIFFERENT TIMING INFORMATION.

WITH RESPECT TO JUST THE CHIP O ON THE BOTTOM, CLOCK 1 IS RECEIVED FIRST, AND THEN SOME TIME LATER IT'S GETTING INFORMATION, A DIFFERENT TIMING INFORMATION, FROM CLOCK 2.

IN CONTRAST, IN THE ACCUSED HYNIX DEVICES, THE TIMING INFORMATION IS ONLY BEING PROVIDED WHERE THE TWO CLOCKS CROSS, AND IT DOESN'T MATTER THAT THAT CROSSING POINT MIGHT VARY OR FLUCTUATE FROM WHAT'S IDEAL.

THE POINT IS THAT AT EACH INSTANCE WHERE THE CLOCKS ARE BEING SAMPLED, THEY'RE BEING SAMPLED TOGETHER AND THERE'S IDENTICAL TIMING INFORMATION.

IT'S NOT SAMPLING TWO DIFFERENT CLOCKS AT TWO DIFFERENT TIMES. IT'S NOT SAMPLING OR LOOKING AT THE COMPLEMENTARY CLOCKS.

IF I CAN BACK UP HERE, IT'S NOT LOOKING AT, FOR EXAMPLE, IF WE WERE TO LOOK AT, MOVE ONE OF THESE ARROWS TO THE RIGHT WHERE CLOCK BAR, WHICH IS DEPICTED IN DOTTED GREEN LINE, IS LOW AND WHERE

CLOCK IS HIGH, WHICH IS BLUE, THE DEVICES THAT ARE ACCUSED OF INFRINGEMENT HERE ARE NOT SAMPLING INFORMATION AND TAKING THE SIGNALS FROM THOSE CLOCKS AT ANY OTHER POINT OTHER THAN THE CROSSING POINTS.

NOW, IF THE CLOCKS BEING SAMPLED IN THE MIDDLE OF THOSE SIGNALS ARE CLOCK WAS HIGH AND CLOCK BAR WAS LOW, THAT WOULD POTENTIALLY BE PROVIDING A DIFFERENT TIMING INFORMATION BECAUSE AT THAT POINT ONE IS A LOGIC HIGH AND ONE IS A LOGIC LOW.

BUT WHAT, IN FACT, IS GOING ON IS IT'S THE TWO INFORMATION AT THE CROSSING POINTS THAT ARE PROVIDING THE CLOCK INFORMATION, OR I SHOULD SAY THE IDENTICAL TIMING INFORMATION.

THE COURT: AREN'T YOU, IN ESSENCE, THOUGH, WHEN YOU PICK THE CROSSING POINT, COMPARING CLOCK 1 AND CLOCK 2?

MR. JONES: YES, THEY ARE BEING COMPARED, YES.

BUT THEY'RE STILL PROVIDING THE SAME INFORMATION. I MEAN, IT'S, IN ESSENCE, INSTEAD OF READING JUST THE FALLING EDGE OF ONE CLOCK, OR JUST THE RISING EDGE OF ONE CLOCK TO DENOTE YOUR TIMING INFORMATION, OR IN CONTRAST TO WHAT RAMBUS IS

DOING, LOOKING AT THE RISING EDGE OF ONE CLOCK AND THE FALLING EDGE, OR THE RISING EDGE OF ANOTHER CLOCK AT ANOTHER TIME, THIS TIMING INFORMATION IS ALWAYS THE CROSSING POINT.

THE COURT: I UNDERSTAND THAT, AND I SEE HOW IT'S QUITE DIFFERENT IN SOME WAYS THAN RAMBUS'S.

BUT IT IS COMPARING TWO CLOCKS, THE RISING ON ONE AND THE GOING DOWN ON THE OTHER, AND COMPARING THEM TO FIND OUT WHERE THEY CROSS.

MR. JONES: WELL, I THINK, YOUR HONOR, WHAT'S HAPPENING -- WELL, THAT IS A WAY TO CHARACTERIZE IT.

BUT WHAT'S HAPPENING IS THE INFORMATION THAT'S BEING DERIVED FROM THE SIGNALS IS ALWAYS BEING DERIVED AT THAT CROSSING POINT.

THE COURT: RIGHT.

MR. JONES: AND THAT'S ONE BIT OF INFORMATION AT THAT PARTICULAR TIME IN CROSSING, AND THAT'S THE TIMING INFORMATION.

IF WE WERE TO SAMPLE THE CLOCKS AT ANY OTHER POINT IN TIME TO DERIVE TIMING INFORMATION, THEN THEY WOULD BE PROVIDING DIFFERENT TIMING INFORMATION.

IF WE WERE GOING TO LOOK AT --

THE COURT: SO IF WE SAMPLED AT THE PEAK, AT THE TOP AND THE BOTTOM AND TOOK AN AVERAGE, THAT WOULD BE SAMPLING THAT WOULD MEET THE LIMITATION?

MR. JONES: I'M NOT SURE I'M FOLLOWING.

I GUESS WHAT I'M SAYING IS IF YOUR REFERENCE POINT IS WHETHER YOUR CLOCKS ARE HIGH OR LOW AND YOU WERE TO SAMPLE -- AND YOUR CRITERIA WAS, WELL, I WANT TO KNOW AT A GIVEN PARTICULAR TIME, IS THE CLOCK HIGH, IS ONE CLOCK HIGH AND IS ONE CLOCK LOW AND WHERE THOSE POINTS IN TIME ARE, THEN, YES, THAT WOULD PROBABLY MEET THE LIMITATION.

THE COURT: IN OTHER WORDS, IF YOU SAMPLE ANYWHERE OTHER THAN THE CROSSING POINT?

MR. JONES: YES, I -- WELL, NOT NECESSARILY, YOUR HONOR.

I GUESS THE OTHER THING TO EMPHASIZE IS THAT ALTHOUGH THEY ARE IDEALIZED, THEY'RE ESSENTIALLY MIRROR IMAGES OF ONE ANOTHER, INVERSES, SO THAT THE -- IN THE IDEAL SITUATION, THE RISING EDGE OF ONE CLOCK IS GOING TO BEGIN WHEN THE FALLING EDGE OF ANOTHER ONE ALSO TAKES PLACE.

SO IF YOU WERE TO LOOK AT THAT PARTICULAR POINT IN TIME, THE INFORMATION, IT'S JUST OF MATTER OF WHETHER YOU'RE SEEING A LOGICAL HIGH OR A LOGICAL LOW.

NOW, THE REASON THE CROSSING POINT IS TAKEN IS BECAUSE PROBABLY, IN PART, ALTHOUGH I -- THIS IS IDEALIZED. IT'S NOT NECESSARILY THE BEST PLACE TO SAMPLE THE CLOCK SIGNALS.

AND SO IF YOU TAKE THE CLOCK AND USE, AS YOUR REFERENCE POINT, THE CROSSING POINT, THAT PROVIDES A MORE EFFECTIVE WAY OF, OF TIMING THE CLOCK.

IF YOU IMAGINE, FOR ONCE, IF YOU TOOK AWAY, IN THIS EXAMPLE, CLOCK BAR, WHICH IS IDENTIFIED WITH THE DOTTED GREEN LINES, YOUR OPTION HERE, AND REALLY THIS IS NO DIFFERENT, IS THAT YOU WOULD BE SAMPLING -- INSTEAD OF SAMPLING AT THE CROSSING POINT, YOU'RE ESSENTIALLY SAMPLING AT THE RISING EDGE OF CLOCK ON EVERY PULSE, OR THE RISING EDGE OF CLOCK HERE, AND IN THE MIDDLE YOU'RE SAMPLING THE FALLING EDGE OF CLOCK, AND IN THE LAST EXAMPLE YOU'RE SAMPLING THE RISING EDGE OF CLOCK.

NOW, THE ADDITION OF CLOCK BAR MAY PROVIDE FOR ADDITIONAL AND MORE PRECISE TIMING.

BUT THE INFORMATION AND THE POINTS AT WHICH THAT INFORMATION IS BEING TAKEN, THAT TIMING INFORMATION, HAS NOT CHANGED.

THE COURT: OKAY. ALL RIGHT.

MR. DETRE: YOUR HONOR, I THINK THAT

HYNIX IS REALLY MUDDLING TOGETHER TWO DIFFERENT POINTS HERE, AND I DON'T THINK EITHER POINT REALLY HOLDS UP.

AND ONE POINT SEEMS TO BE THAT THEIR COMPLEMENTARY CLOCKS DON'T PROVIDE DIFFERENT TIMING INFORMATION BECAUSE THEY'RE JUST PROVIDING A SINGLE TIMING REFERENCE TO THE DEVICE AT THE CROSSING POINT.

THE OTHER POINT SEEMS TO BE THAT THEY'VE GOT THESE COMPLEMENTARY CLOCKS THAT ARE JUST MIRROR IMAGES OF ONE ANOTHER AND THAT MEANS THEY DON'T PROVIDE DIFFERENT TIMING INFORMATION.

SO I'D LIKE TO TAKE THOSE IN ORDER.

WITH RESPECT TO THE FIRST POINT, THAT BECAUSE YOU'RE TAKING THESE TWO DIFFERENT CLOCK SIGNALS, THEY ARE DIFFERENT, ONE -- EVEN IF THEY WERE PERFECTLY COMPLEMENTARY, ONE HAS THE RISING EDGE AND THE OTHER HAS THE FALLING EDGE AND THAT'S WHAT ENABLES YOU TO FIND THE CROSSING POINT.

IF THEY WERE IDENTICAL CLOCK SIGNALS, OF COURSE, YOU COULD NOT FIND THE CROSSING POINT.

THEY -- THIS IS ESSENTIALLY WHAT GOES ON IN THE RAMBUS PREFERRED EMBODIMENT THAT MR. JONES WAS DOING HIS BEST TO DISTINGUISH.

IT'S TRUE THAT THE RAMBUS PREFERRED

EMBODIMENT TAKES TWO DIFFERENT CLOCK SIGNALS AND FINDS THE MID-POINT, WHICH IT THEN USES AS A TIMING REFERENCE.

THE HYNIX DEVICES TAKE TWO DIFFERENT CLOCK SIGNALS AND FINDS THE CROSSING POINT AND USES THAT AS THE TIMING REFERENCE.

IN BOTH CASES, YOU TAKE TWO DIFFERENT CLOCK SIGNALS PROVIDING DIFFERENT INFORMATION AND COMBINE THEM IN ORDER TO PROVIDE A TIMING REFERENCE TO THE DEVICE.

THAT'S HYNIX'S FIRST POINT.

THE OTHER POINT SEEMS TO BE THAT COMPLEMENTARY CLOCKS DON'T REALLY PROVIDE DIFFERENT TIMING INFORMATION BECAUSE THEY'RE JUST MIRROR IMAGES.

AS I MENTIONED, THEY DO PROVIDE DIFFERENT TIMING INFORMATION. THAT'S WHAT ALLOWS YOU TO FIND THE CROSSING POINT.

THE SECOND POINT, IT'S CERTAINLY NOT THE CASE THAT COMPLEMENTARY CLOCKS IN THE ABSTRACT DON'T PROVIDE DIFFERENT TIMING INFORMATION.

AS YOU MAY RECALL FROM THE DISCUSSION YESTERDAY, RAMBUS'S EMBODIMENT ALSO HAS TWO INTERNAL CLOCKS WHICH ARE COMPLEMENTS OF ONE ANOTHER.

AND YOU MAY RECALL MR. JONES SAYING YESTERDAY, WELL, HYNIX AGREED TO THE CONSTRUCTION OF INTERNAL CLOCKS WITHOUT THE DIFFERENT TIMING INFORMATION LIMITATION BECAUSE THOSE TWO CLOCKS ARE JUST COMPLEMENTS OF ONE ANOTHER, THEY DON'T PROVIDE DIFFERENT TIMING INFORMATION.

HYNIX'S EXPERT, HOWEVER, IS OF A DIFFERENT VIEW. MR. TAYLOR, IN HIS DEPOSITION -- WE DISCUSSED THOSE INTERNAL CLOCKS AND THAT THEY WERE COMPLEMENTS OF ONE ANOTHER IN THE RAMBUS PREFERRED EMBODIMENT.

AND THEN I ASKED MR. TAYLOR, THIS IS ON PAGE 51 OF HIS DEPOSITION AT LINE 20, "OKAY. SO THAT -- IS IT FAIR TO SAY, THEN, THAT THE TWO INTERNAL CLOCKS IN THE RAMBUS PREFERRED EMBODIMENT, WHEN YOU CONSIDER THEM IN CONNECTION WITH THE OUTPUTTING OF DATA, PROVIDE DIFFERENT TIMING INFORMATION?"

AND MR. TAYLOR ANSWERED, "YES."

SO THERE'S AN EXAMPLE OF TWO COMPLEMENTARY CLOCKS THAT HYNIX APPARENTLY AGREES PROVIDE DIFFERENT TIMING INFORMATION.

THE THIRD POINT I WANT TO MAKE IS, RELATES TO THIS IDEA THAT, IN FACT, CLOCKS, IN PRACTICE, WILL NOT BE PERFECTLY COMPLEMENTARY.

HYNIX'S DATA SHEET PROVIDES FOR A MARGIN. IF THE CLOCKS WERE PERFECTLY COMPLEMENTARY, THE CROSSING POINT WILL ALWAYS APPEAR ON THAT MID-VOLTAGE LINE AS SHOWN IN MR. JONES' GRAPHIC.

IN HYNIX'S DATA SHEETS, IT PROVIDES FOR A MARGIN OF PLUS OR MINUS TWO VOLTS WHERE THAT CROSSING POINT CAN APPEAR AND STILL SATISFY THE REQUIREMENTS OF THE DEVICE.

NOW, IF WE COULD PULL UP THAT MICRON TECHNICAL NOTE, AND GO TO THE -- TO THAT PAGE. AND CAN WE BLOW UP THE FIGURE?

THIS IS ACTUALLY A FIGURE FROM A MICRON TECHNICAL NOTE, BUT I JUST WANT TO USE IT FOR ILLUSTRATIVE PURPOSES.

I SHOWED THIS TO MR. TAYLOR AT HIS DEPOSITION AND HE AGREED THAT THIS BASICALLY ILLUSTRATED THAT POINT OF THE MARGIN THAT YOU COULD HAVE WHERE THE CROSSING POINTS ACTUALLY ARE, FOR NON-IDEALIZED CLOCKS, AND THEY COULD -- HERE'S A CROSSING POINT THAT'S .2 VOLTS BELOW THE MID-LINE.

THE COURT: OKAY. I UNDERSTAND THAT.

MR. DETRE: OKAY. AND AS MR. JONES MENTIONED, HYNIX USES THESE MORE OR LESS COMPLEMENTARY CLOCKS IN ORDER TO ACHIEVE MORE PRECISE TIMING.

THE REASON THAT YOU GET MORE PRECISE TIMING IS PRECISELY IN THIS SITUATION WHERE THE CLOCKS DON'T CROSS RIGHT AT THE MID-POINT VOLTAGE.

IF THE CLOCKS WERE CROSSING RIGHT AT THE MID-POINT VOLTAGE, YOU COULD HAVE A SINGLE CLOCK IN THAT MID-LINE VOLTAGE REFERENCE AND GET THE EXACT SAME POINT.

BUT HERE IF YOU USE A SINGLE CLOCK IN THE MID-LINE VOLTAGE REFERENCE WHERE THE CLOCKS ARE NOT PERFECT, USING THIS CROSSING POINT OF THE DIFFERENTIAL CLOCKS, OF THE DIFFERENTIAL CLOCK, OR THE MORE OR LESS COMPLEMENTARY CLOCK SIGNALS ALLOWS FOR A MORE PRECISE, A MORE REGULAR TIMING REFERENCE.

THE COURT: ISN'T THE ESSENTIAL DIFFERENCE BETWEEN YOUR SET UP AND HYNIX'S IS THAT YOU DO YOUR TIMING MEASUREMENTS AT DIFFERENT POINTS IN TIME, WHERE HYNIX DOES IT AT THE SAME TIME?

MR. DETRE: I DON'T THINK SO.

OH, I SEE. IN HYNIX'S DEVICES, HYNIX'S DEVICES RECEIVE THE COMPLEMENTARY --

THE COURT: RIGHT.

MR. DETRE: -- CLOCKS AT ESSENTIALLY THE SAME TIME AND THEN CALCULATE THE CROSSING POINT, AND THE RAMBUS PREFERRED EMBODIMENT RECEIVES THE

EARLY AND LATE CLOCKS --

THE COURT: RIGHT.

MR. DETRE: -- AT -- WELL, I -- I MEAN, I THINK IN EACH CASE THE -- I MEAN, THESE ARE CONTINUOUS CLOCK SIGNALS THAT ARE BEING SUPPLIED TO THE DEVICE.

IN EACH CASE IN THE RAMBUS PREFERRED EMBODIMENT, THE DEVICES ARE RECEIVING THIS EARLY CLOCK, IT'S A CLOCK SIGNAL GOING UP AND DOWN, AND THEY'RE RECEIVING THE LATE CLOCK AND CALCULATING THAT MID-POINT.

IN THE HYNIX DEVICES, THEY'RE RECEIVING THE, THE TWO COMPLEMENTARY CLOCK SIGNALS CONTINUOUSLY IN THE SAME WAY AND CALCULATING THE CROSS POINTS, SO I DON'T THINK THAT THAT'S REALLY A DISTINCTION.

FINALLY, THE LAST POINT I WANT TO MAKE ABOUT THIS IS THAT, IN FACT, THE PREFERRED EMBODIMENT IN THE RAMBUS PATENT ALSO INCLUDES, AS A SPECIAL CASE, THE SITUATION WHERE THAT EARLY AND LATE CLOCK WILL, IN FACT, BE COMPLEMENTS OF ONE ANOTHER.

AND THAT'S BECAUSE THE EARLY CLOCK COMES IN, THE LATE CLOCK COMES IN AT SOME POINT LATER, PHASE SHIFTED, AND IF IT'S PHASE SHIFTED BY JUST

THE RIGHT AMOUNT, THEN THE RISING EDGE OF THE EARLY CLOCK WILL LINE UP WITH THE FALLING EDGE OF THE LATE CLOCK AND THERE WILL BE COMPLEMENTARY CLOCK SIGNALS COMING IN.

HYNIX, IN ITS -- WE POINTED THIS OUT AND HYNIX RESPONDED, WELL, YOU KNOW, THIS IS JUST SOME MADE UP EXAMPLE ON RAMBUS'S PART BECAUSE IN THAT CASE THERE WOULD BE EXCESSIVE DELAY AND IT'S NOT REALLY A SITUATION CONTEMPLATED BY THE PATENT.

THE COURT: RIGHT.

MR. DETRE: AND I DISAGREE WITH THAT AND I'D LIKE TO EXPLAIN WHY.

IF WE COULD GO TO THE '263 PATENT AT PAGE 25. COLUMN 17, RIGHT AT THE BOTTOM. BLOW IT UP. THAT'S FINE. WHERE YOU WERE BEFORE, THAT'S FINE. EITHER WAY.

AND THIS IS TALKING ABOUT, IN THE PREFERRED EMBODIMENT, WHAT THE -- YOU WANT TO KEEP THE BUS SHORT IN THE RAMBUS PREFERRED EMBODIMENT BECAUSE THAT'S WHAT ALLOWS FOR HIGH-SPEED COMMUNICATION WITHOUT TOO MUCH OF A TIME LAG AMONG DEVICES.

AND YOU'VE GOT A 500 MEGAHERTZ CLOCK IN THE PREFERRED EMBODIMENT WHICH, AS THE SPECIFICATION NOTES HERE, CORRESPONDS TO TWO

NANOSECOND BUS CYCLES, FOUR NANOSECOND BUS CYCLES, AND THERE ARE TWO BUS CYCLES PER CLOCK CYCLE.

AND THEN IT POINTS OUT, "TO OPERATE AT A TWO NANOSECOND DATA RATE," I'M READING AT LINE 63, "THE TRANSIT TIME ON THE BUS SHOULD PREFERABLY BE KEPT UNDER ONE NANOSECOND TO LEAVE ONE NANOSECOND FOR THE SETUP AND HOLD TIME OF THE INPUT RECEIVERS."

IF WE -- LET'S GO UP TO THE TOP OF THE NEXT COLUMN, COLUMN 18. JUST THAT, YEAH, VERY LITTLE BIT. THERE WE GO.

IT NOTES THAT YOU CAN HAVE LOWER PERFORMANCE SYSTEMS WITH LONGER LINES, BUT IN THE VERY PREFERRED EMBODIMENT, YOU WANT TO KEEP THAT BUS TRANSIT TIME DOWN TO ONE NANOSECOND.

SO I'D LIKE TO JUST BRIEFLY DISCUSS WHAT THAT MEANS ABOUT WHERE THE EARLY CLOCKS AND THE LATE CLOCKS SHOW UP.

COULD WE GO TO GRAPHIC NUMBER 67?

AND THIS IS JUST A FIGURE FROM THE PATENT THAT WE'VE MODIFIED SLIGHTLY. I THINK IT'S FIGURE 2. YEAH, IT'S FIGURE 2 SHOWING, SHOWING THE PREFERRED EMBODIMENT OF THE BUS.

AND WE'VE JUST -- WE'RE ASSUMING, IT'S NOT NECESSARILY THE CASE, BUT WE'RE ASSUMING FOR

THIS EXAMPLE THAT THE CLOCK, CLOCK 1 AND CLOCK 2 AS SHOWN IN THIS PREFERRED EMBODIMENT, GO ALONG BUS LINES OF ESSENTIALLY THE SAME LENGTH AS THE REST OF THE BUS.

AND WE'VE MODIFIED THE FIGURE TO PUT IN THAT CLOCK LOOP AT THE LEFT-HAND SIDE OF CLOCK 1 AND CLOCK 2.

NOW, IN THE PREFERRED LENGTH OF THE BUS DESCRIBED IN THE PATENT SPECIFICATION I JUST READ, IT'S THE TRANSIT TIME ON THE BUS, AND THAT'S BETWEEN DEVICES. THAT'S ONE-WAY TRANSIT TIME THAT SHOULD BE KEPT TO ONE NANOSECOND.

THAT MEANS THAT THE CLOCK LOOP TRANSIT TIME THAT THE CLOCK GOES FROM ONE AND THEN LOOPS BACK AROUND IS TWO NANOSECONDS.

IN THE PREFERRED EMBODIMENT WE'VE GOT A 250 MEGAHERTZ CLOCK, AND THAT CORRESPONDS AS SHOWN IN THE BOTTOM, WE'VE ADDED THIS TO THE FIGURE, A FOUR NANOSECOND PERIOD, A FOUR NANOSECOND CYCLE TIME.

AND IF YOU'VE GOT IN THIS, IN WHAT'S DESCRIBED AS THE PREFERRED LENGTH OF THE BUS IN THE PATENT SPECIFICATION, IF YOU'VE GOT DEVICES PRECISELY AT ONE END GETTING THE EARLY CLOCK AS EARLY AS CAN BE, AND AT THE OTHER END GETTING THE

LATE CLOCK AS LATE AS CAN BE, YOU'VE SHIFTED, BY TWO NANOSECONDS PRECISELY. THAT'S THE CLOCK LOOP TRANSIT TIME.

AND YOU MOVE THAT CLOCK OVER BY TWO NANOSECONDS AND YOU'VE GOT YOUR COMPLEMENTARY CLOCKS.

SO NOTHING MADE UP ABOUT THAT EXAMPLE. IT'S A PRECISE KIND OF EXAMPLE THAT YOU CAN HAVE IF YOU FOLLOW THE INSTRUCTIONS IN THE PATENT FOR THE VERY PREFERRED EMBODIMENT.

THAT'S ALL I HAVE TO SAY ABOUT THIS ISSUE.

THE COURT: OKAY. DO YOU HAVE ANYTHING FURTHER ON THAT? YOU DON'T NEED TO, I JUST --

MR. JONES: WELL, SOMETIMES YOU FEEL COMPELLED TO.

BUT THE -- YOU KNOW, THERE ARE TWO MAKE BELIEVE, OR CONCOCTED POSSIBILITIES FROM THE RAMBUS PERSPECTIVE WHEN THEY TALK ABOUT WHAT COULD BE, AND ONE MR. DETRE JUST SPOKE ABOUT, WHICH IS IF YOU MAKE THE BUS LONG ENOUGH AND ONE CHIP THAT'S CLOSE ENOUGH TO THE CLOCK GENERATOR SUCH THAT BY THE TIME THE EARLY CLOCK BECOMES THE LATE CLOCK, THAT ONE CHIP IS GOING TO SEE A COMPLEMENTARY CLOCK.

THE OTHER ONE, WHICH WASN'T SUGGESTED

TODAY, OR AT LEAST WASN'T MENTIONED IN THE LAST FEW MOMENTS, WAS -- AND THEN THE OTHER INSTANCE IS, OKAY, WHAT IF YOU TOOK ONE OF THESE DEVICES AND YOU PUT IT AT THE U-TURN OF THE CLOCK SO THAT AT THAT POINT CLOCK 1 AND CLOCK 2 ARE PROVIDING THE SAME INFORMATION?

NOW, THIS KIND OF DOVETAILS INTO WHY HYNIX PROFFERED THE CONSTRUCTION IT DID, AND THE ALTERNATE ARGUMENTS THAT HAVE BEEN PRESENTED IN OUR MOTION, OR ALTERNATE GROUNDS, AS TO WHY YOU NEED TWO DIFFERENT TIMING INFORMATIONS PROVIDED BY THESE CLOCKS, AND THAT IS THAT THOSE TWO MAKE UP, MADE UP OR CONCOCTED HYPOTHETICALS ARE NOT DISCLOSED WITHIN THE SPECIFICATION.

THERE'S NO SUGGESTION THAT RECEIVING BOTH CLOCKS AT THE SAME TIME AND HAVING THEM COMPLEMENTARY, IN FACT, ACCOUNTS FOR HAVING TWO EXTERNAL CLOCKS PROVIDING TWO DIFFERENT TIMING INFORMATIONS.

AND THE POSSIBILITY OF PUTTING ONE AT THE END AND ONE AT THE U-TURN IS NOWHERE WITHIN THE SPECIFICATION, NOR WITHIN THE FILE HISTORY, AND NOWHERE EVEN WITHIN THE CLAIMS AS ORIGINALLY FILED.

THE COURT: ALL RIGHT.

YOU WANTED TO MENTION SOMETHING ABOUT

SYNCHRONOUS MEMORY DEVICE?

MR. DETRE: YES, YOUR HONOR, AND I'LL BE BRIEF BECAUSE I -- IT IS FAIRLY WELL LAID OUT IN OUR PAPERS, BUT THERE ARE A COUPLE OF POINTS I'D LIKE TO STRESS, ONE OF WHICH IS NOT EXPRESSLY IN OUR PAPERS.

ON SYNCHRONOUS MEMORY DEVICE, HYNIX ARGUES ESSENTIALLY THAT ALL OF RAMBUS'S CLAIMS INVOLVING SYNCHRONOUS MEMORY DEVICE NEED TO BE RESTRICTED TO THE PREFERRED CLOCK DISTRIBUTION SCHEME THAT WE'VE BEEN DISCUSSING, THE EARLY CLOCK AND A LATE CLOCK AND CALCULATING THE MID-POINT IS ESSENTIALLY THE USUAL ARGUMENT BECAUSE THEY SAY THAT'S THE ONLY TYPE OF CLOCK DISTRIBUTION SCHEME DESCRIBED IN THE PATENTS.

I WANT TO MAKE THE POINT -- TO SOME EXTENT, THIS OVERLAPS OUR OTHER ARGUMENTS THAT A PERSON OF ORDINARY SKILL WOULD UNDERSTAND THAT DISTINCT INVENTIONS COULD BE USED WITH OTHER WELL-KNOWN CLOCK DISTRIBUTION SCHEMES.

IN THIS CASE ALSO, THE PATENT SPECIFICATION DISCUSSES INVENTIONS USING A CLOCK BEFORE THE PREFERRED CLOCK DISTRIBUTION SCHEME IS ACTUALLY LAID OUT.

AND FIGURE 14, FOR EXAMPLE, IN THE

PATENT, WHICH WE MENTION IN OUR PAPERS, SHOWS A CLOCK WHICH GOES TO A MASTER AND TWO DEVICES, IT MUST BE A SYSTEM CLOCK, WHICH IS DISCUSSED BEFORE THE PREFERRED CLOCK DISTRIBUTION SCHEME IS DISCUSSED.

AND THEN --

COULD WE GO TO THE '263 PATENT. I DON'T HAVE A PAGE NUMBER. I WANT TO GO TO COLUMN 18. OH, HOLD ON. I CAN TELL YOU WHAT THAT IS. IT IS PAGE 25.

AND -- OH, THAT'S WHERE WE WERE BEFORE. IF WE COULD GO TO THE CLOCKING SECTION NEAR THE BOTTOM OF THE RIGHT-HAND COLUMN.

SO AFTER DISCUSSING VARIOUS DISTINCT INVENTIONS OPERATING WITH A CLOCK, THEN THE RAMBUS SPECIFICATION TURNS TO THIS DISTINCT INVENTION.

"CLOCKING. CLOCKING A HIGH SPEED BUS ACCURATELY WITHOUT INTRODUCING ERROR DUE TO PROPAGATION DELAYS CAN BE IMPLEMENTED BY HAVING EACH DEVICE MONITOR TWO BUS CLOCK SIGNALS AND THEN DERIVE INTERNALLY A DEVICE CLOCK, THE TRUE SYSTEM CLOCK."

I THINK HERE THE SPECIFICATION IS VERY CLEAR THAT THIS IS A DISTINCT INVENTION THAT YOU CAN USE IF YOU WEREN'T GOING TO USE THE PRIOR ART

CLOCK DISTRIBUTION SCHEMES WELL-KNOWN IN THE ART.

AND THE LAST POINT I WANT TO MAKE ABOUT THAT IS THAT THIS WAS RECOGNIZED IN CONNECTION WITH THE ORIGINAL RESTRICTION REQUIREMENT, THAT THIS WAS A DISTINCT INVENTION BY, BY THE EXAMINER AT THE PTO.

AND IF WE COULD PULL UP THE ORIGINAL RESTRICTION REQUIREMENT, WHICH WAS ATTACHED TO THIS, TO ONE OF MR. BROWN'S DECLARATIONS AS EXHIBIT 83.

THERE IT IS. AND LET'S GO TO PAGE 4. AND COULD YOU BLOW UP STARTING AROUND THE MIDDLE. ALL RIGHT. LET'S GO DOWN JUST A FEW MORE LINES. STOP. LET'S GO UP A FEW MORE LINES, THEN WE'LL GO DOWN.

ONE OF THE RESTRICTION REQUIREMENTS IMPOSED HERE WAS BETWEEN GROUP I, WHICH INCLUDED CLAIMS 1 TO 45 AND SOME OTHER CLAIMS IN THE PATENT, AND GROUP III.

AND IN THE ORIGINAL RESTRICTION REQUIREMENT, THE EXAMINER SAID, "GROUP I RELATES TO A MEMORY AND BUS SUBSYSTEM, INCLUDING ADDRESS REGISTER, TRANSCEIVERS, AND MEMORY SECTIONS, A, AND GENERAL MENTION OF TIMING, BBR."

THEN IT GOES ON. "GROUP III IS THE

SUBCOMBINATION, PSP, WHICH IS A SPECIFIC CLOCKING AND TIMING SCHEME."

AND IF YOU LOOK AT GROUP III, IT BEGINS WITH CLAIM 73, AND IF YOU LOOK UP ORIGINAL CLAIM 73, YOU WILL SEE ESSENTIALLY THIS PREFERRED RAMBUS CLOCK DISTRIBUTION SCHEME OF THE EARLY AND LATE CLOCKS AND CALCULATING THE MID-POINT.

AND THEN THE EXAMINER GOES ON. "SINCE CLAIMS TO BOTH THE COMBINATION AND SUBCOMBINATION ARE PRESENTED AND ASSUMED TO BE PATENTABLE, THE OMISSION OF THE DETAILS OF THE CLAIMED SUBCOMBINATION IN THE COMBINATION ABBR, IS EVIDENCE THAT THE PATENTABILITY OF THE COMBINATION DOES NOT RELY ON THE DETAILS OF THE SPECIFIC SUBCOMBINATION."

THIS IS AN EXPLICIT RECOGNITION BY THE EXAMINER THAT YOU, THAT THE GROUP I CLAIMS, WHICH HAD ONLY A GENERAL MENTION OF TIMING, DID NOT HAVE TO USE THE PREFERRED CLOCK DISTRIBUTION SCHEME WHICH WAS CLAIMED SEPARATELY AND WHICH WAS MADE SUBJECT TO A RESTRICTION REQUIREMENT.

THE COURT: WHAT'S YOUR COMMENT, IF ANY, WITH RESPECT TO THE SYNCHRONOUS MEMORY DEVICE DEFINITION THAT I GAVE YOU TODAY?

MR. DETRE: WE WOULD LIKE THE

OPPORTUNITY, YOUR HONOR, TO SUBMIT A PAPER ON THAT ON FRIDAY.

THE COURT: OKAY.

MR. DETRE: AND YOUR HONOR HAD MENTIONED THAT --

THE COURT: YEAH. LET'S LET -- MR. BROWN, DID YOU HAVE ANYTHING ELSE BEFORE WE BREAK?

MR. BROWN: YES, I DID, YOUR HONOR.

RAMBUS MISCONSTRUES OUR ARGUMENT ON THE SYNCHRONOUS MEMORY, ON THIS SYNCHRONOUS MEMORY DEVICE, AND WHETHER OR NOT THIS PARTICULAR CLOCKING SCHEME IS SOMETHING THAT COULD BE SEPARATELY PATENTABLE REALLY MISSES THE POINT ENTIRELY.

THE ONLY CLOCKING SCHEME WHICH IS DISCLOSED IN THE PATENT IS THIS EARLY CLOCK, LATE CLOCK SCHEME.

SO THAT THE ONLY -- THE ONLY -- THE ONLY SCHEME, THE ONLY CLOCKING SCHEME IS ONE WHERE THERE ARE TWO CLOCKS WITH DIFFERENT TIMING INFORMATION, AND THERE ARE NO OPERATIONS OF THE INTERNAL, THE INPUTS, THE OUTPUTS THAT TAKE PLACE WITH RESPECT TO ONE OF THOSE EXTERNAL CLOCKS.

AND IN OUR INITIAL VIEW, WE THINK THAT THE PROPOSED DEFINITION THAT YOU POSTED ON THE

BOARD IS FINE ON SYNCHRONOUS MEMORY DEVICE.

BUT IT ONLY RECITES ONE EXTERNAL CLOCK, AND THE DEFINITION -- WE AGREE THAT IT'S AN APPROPRIATE MARKMAN DEFINITION, BUT BASICALLY THERE'S NO SUPPORT FOR IT IN THE RAMBUS DISCLOSURE BECAUSE THERE'S NO EMBODIMENT OF ANY CLOCKING SCHEME IN THE RAMBUS DISCLOSURE THAT HAD, THAT DOES INPUTS AND OUTPUTS OR REFERENCES ANY OPERATIONS WITH RESPECT TO JUST ONE EXTERNAL CLOCK.

THE COURT: OKAY.

MR. BROWN: OKAY. AND YOU MENTIONED THAT THERE WERE SOME OTHER ISSUES THAT YOU WANTED ADDITIONAL INFORMATION ON.

THE COURT: MOST OF IT HAS BEEN COVERED, BUT I WOULD LIKE YOUR RESPECTIVE COMMENTS ON MY REVISED PROPOSED SYNCHRONIZED MEMORY DEVICE; AND I THINK IT WOULD BE HELPFUL IF YOU BOTH DEFINE FOR ME A PACKET.

I THINK THAT'S IT.

MR. DETRE: YOUR HONOR, WOULD YOU LIKE THOSE BOTH BY FRIDAY?

THE COURT: IF YOU COULD.

MR. BROWN: OKAY.

MR. DETRE: WE WILL.

THE COURT: OKAY.

MR. BROWN: THANK YOU, YOUR HONOR.
THE COURT: THANK YOU.
MR. DETRE: YOUR HONOR, EXCUSE ME. DO I UNDERSTAND, THEN, THAT WE WON'T BE DOING ANYMORE BRIEFING ON READ REQUEST?
THE COURT: UM --
MR. DETRE: IT'S OUR POSITION THAT IT'S BEEN FULLY BRIEFED AND ARGUED AND NO FURTHER BRIEFING IS REQUIRED.
THE COURT: YOU DIDN'T WANT TO DO MORE, DID YOU? OR DID YOU?
MR. BROWN: NO. I JUST THOUGHT THAT IF YOU -- I WAS OFFERING TO DO MORE IF YOU THOUGHT IT WOULD BE OF ANY ASSISTANCE.
THE COURT: I THINK IT'S BEEN PRETTY WELL HASHED OUT.
MR. BROWN: WELL, IT'S BEEN HASHED OUT AT LENGTH, ANYWAY.
THE COURT: OKAY. THANK YOU.
MR. DETRE: THANK YOU, YOUR HONOR.
MR. BROWN: THANK YOU.
(WHEREUPON, THE PROCEEDINGS IN THIS MATTER WERE CONCLUDED.)