

1 UNITED STATES DISTRICT COURT
 2 NORTHERN DISTRICT OF CALIFORNIA
 3 SAN JOSE DIVISION
 4

5 HYNIX SEMICONDUCTOR INC.,) C-00-20905 RMW
 HYNIX SEMICONDUCTOR)
 6 AMERICA INC., HYNIX) SAN JOSE, CALIFORNIA
 SEMICONDUCTOR U.K. LTD.,)
 7 AND HYNIX SEMICONDUCTOR) MARCH 24, 2004
 DEUTSCHLAND GMBH,)
 8) PAGES 1-111
 PLAINTIFFS,)
 9)
 VS.)
 10)
 RAMBUS, INC.,)
 11)
 DEFENDANT.)
 12 _____)

13 TRANSCRIPT OF PROCEEDINGS
 14 BEFORE THE HONORABLE RONALD M. WHYTE
 UNITED STATES DISTRICT JUDGE

15 A P P E A R A N C E S :

16 FOR THE PLAINTIFF: TOWNSEND & TOWNSEND & CREW
 BY: THEODORE G. BROWN, III AND
 17 JORDAN TREND JONES
 379 LYTTON AVENUE
 18 PALO ALTO, CALIFORNIA 94301

19 THELEN, REID & PRIEST
 BY: KENNETH L. NISSLY AND
 20 SUSAN VAN KEULEN
 225 WEST SANTA CLARA STREET
 21 SUITE 1200
 SAN JOSE, CALIFORNIA 95113

22
 23 ALSO PRESENT: DAVID L. TAYLOR

24 APPEARANCES CONTINUED ON NEXT PAGE

25 OFFICIAL COURT REPORTER: LEE-ANNE SHORTRIDGE, CSR, CRR
 CERTIFICATE NUMBER 9595

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APPEARANCES (CONTINUED)

FOR THE DEFENDANT: MUNGER, TOLLES & OLSON
BY: PETER A. DETRE,
GREGORY P. STONE AND
JENNIFER L. POLSE
33 NEW MONTGOMERY STREET
NINETEENTH FLOOR
SAN FRANCISCO, CALIFORNIA 94105

RAMBUS, INC.
PAUL M. ANDERSON, PATENT COUNSEL
4440 EL CAMINO REAL
LOS ALTOS, CALIFORNIA 94022

ALSO PRESENT: ROBERT J. MURPHY

1 SAN JOSE, CALIFORNIA MARCH 24, 2004

2 P R O C E E D I N G S

3 (WHEREUPON, COURT CONVENED AND THE
4 FOLLOWING PROCEEDINGS WERE HELD:)

5 THE CLERK: CALLING CASE C-00-20905,
6 HYNIX SEMICONDUCTOR VERSUS RAMBUS, ON FOR HEARING
7 ON MOTIONS FOR SUMMARY JUDGMENT.

8 COUNSEL, STATE YOUR NAME FOR THE RECORD,
9 YOUR HONOR.

10 MR. BROWN: THEODORE BROWN, YOUR HONOR.
11 FROM TOWNSEND & TOWNSEND & CREW. WITH ME IS MY
12 PARTNER, JORDAN JONES; AND WE HAVE KEN NISSLY AND
13 SUSAN VAN KEULEN FROM THELEN, REID & PRIEST; AND
14 OUR EXPERT, DAVID TAYLOR.

15 MR. DETRE: GOOD AFTERNOON, YOUR HONOR.
16 PETER DETRE, MUNGER, TOLLES & OLSON FOR RAMBUS, AND
17 WITH ME ARE GREG STONE AND JENNIFER POLSE FROM
18 MUNGER, AND ROBERT MADERO, WHO'S DOING OUR
19 GRAPHICS; PAUL ANDERSON FROM RAMBUS; AND
20 MR. MURPHY, OUR EXPERT, IS IN THE AUDIENCE.

21 THE COURT: ALL RIGHT. RATHER THAN
22 INDICATE NOW, BECAUSE I MAY HAVE ADDITIONAL MATTERS
23 THAT I WANT TO ASK FOR BRIEFING ON, MAKE SURE
24 SOMEBODY REMINDS ME AT THE END THAT THERE ARE A
25 COUPLE OF THINGS THAT I WANT SOME FURTHER

1 INFORMATION ON.

2 BUT WITH THAT, HAVE YOU DONE WHAT YOU DID
3 YESTERDAY AND WORK OUT BETWEEN YOURSELVES THE ORDER
4 THAT YOU WANT TO PROCEED ON, OR --

5 MR. BROWN: ACTUALLY, WE DID NOT.

6 THE COURT: OKAY.

7 MR. BROWN: IS THERE AN ORDER THAT YOU
8 WOULD, THAT YOU WOULD LIKE TO HEAR THE ISSUES ON?

9 THE COURT: WELL, WHY DON'T WE GO THROUGH
10 AND SEE IF WE CAN'T FIGURE OUT WHAT MIGHT BE A -- I
11 THINK I'M PARTICULARLY INTERESTED IN THE MOTION
12 DEALING WITH THE BLOCK SIZE INFORMATION, THE
13 OPERATIONS CODE, AND THE SECOND EXTERNAL CLOCK
14 SIGNAL.

15 SO WHY DON'T WE DO THOSE THREE FIRST, AND
16 THEN WE'LL COVER THE OTHERS.

17 MR. BROWN: OKAY.

18 MR. DETRE: YOUR HONOR, I THINK YOU MEAN
19 HYNIX'S MOTIONS, BECAUSE RAMBUS ALSO HAS A MOTION
20 FOR SUMMARY JUDGMENT WHICH DISCUSSES AT LEAST A
21 COUPLE OF THOSE.

22 THE COURT: RIGHT. I WAS NOT TRYING TO
23 LIMIT IT TO EITHER YOUR MOTION OR THEIR MOTION.

24 MR. DETRE: OH, I SEE.

25 THE COURT: THOSE ARE THE ISSUES, THE

1 ONES THAT INVOLVE ISSUES PERTAINING TO THOSE ITEMS.

2 MR. DETRE: OKAY. DO YOU HAVE A
3 PREFERENCE AS TO WHETHER WE DO RAMBUS'S MOTION
4 FIRST OR HYNIX'S MOTIONS?

5 THE COURT: SHOULDN'T WE DO THEM AT THE
6 SAME TIME TO THE EXTENT THAT THEY OVERLAP?

7 MR. BROWN: I'LL ADDRESS BLOCK SIZE, YOUR
8 HONOR.

9 THE COURT: OKAY. IS THAT OKAY THAT HE
10 GOES FIRST ON BLOCK SIZE?

11 MR. DETRE: THAT WOULD BE FINE, YOUR
12 HONOR. I THINK ACTUALLY, IN THAT CASE, VERY
13 SIMILAR ISSUES ARE RAISED BY --

14 MR. BROWN: BOTH MOTIONS.

15 MR. DETRE: -- BOTH MOTIONS.

16 THE COURT: OKAY.

17 MR. BROWN: IT'LL TAKE ME JUST A MINUTE,
18 YOUR HONOR.

19 THE COURT: OKAY.

20 MR. BROWN: OKAY, BLOCK SIZE INFORMATION.

21 AND BECAUSE I HAVE NOT COMPLETELY
22 REVAMPED THIS FROM WHAT I HAD IN MIND YESTERDAY, OR
23 IN VIEW OF YESTERDAY'S DISCUSSION, WHAT I'M GOING
24 TO DO, I'VE PRESENTED THE TWO CLAIM CONSTRUCTIONS
25 HERE, BUT FROM THE TENTATIVE RULING, BASICALLY IT

1 APPEARS, AT LEAST TENTATIVELY, THAT THE COURT'S
2 INCLINED TO ADOPT SOMETHING THAT'S PRETTY SIMILAR
3 TO HYNIX'S CONSTRUCTION, SO I'M MOSTLY GOING TO
4 TALK ABOUT THAT.

5 THERE ARE TWO REASONS WHY HYNIX, WHY THE
6 ACCUSED PRODUCTS DO NOT USE BLOCK SIZE INFORMATION
7 UNDER THIS CONSTRUCTION.

8 ONE OF THOSE REASONS ALSO APPLIES TO THE
9 PROPOSED RAMBUS CONSTRUCTION.

10 FIRST, THE BLOCK SIZE INFORMATION, OR
11 WHAT -- MORE PROPERLY WHAT RAMBUS SAYS REPRESENTS
12 BLOCK SIZE INFORMATION IN THE ACCUSED PRODUCTS DOES
13 NOT TRANSFER, DOES NOT SPECIFY OR REPRESENT THE
14 TOTAL AMOUNT OF DATA THAT IS TO BE TRANSFERRED ON
15 THE BUS, AND IT DOESN'T EVEN SPECIFY A QUANTITY OF
16 DATA WHICH IS TO BE TRANSFERRED ON THE BUS OR
17 TRANSFERRED DURING A MEMORY OPERATION.

18 AND I'M GOING TO GO BACK HERE, THIS IS A
19 LITTLE BIT ON CLAIM CONSTRUCTION ISSUES, AND THE
20 COURT WILL RECALL THAT BLOCK SIZE INFORMATION,
21 WHICH IS DISCLOSED IN THE PATENT, IS A FIELD WITHIN
22 THE REQUEST PACKET THAT SPECIFIES THE AMOUNT OF
23 DATA, OR THE SIZE OF THE BLOCK TO BE TRANSFERRED IN
24 RESPONSE TO THE REQUEST.

25 AND WHAT I WANT TO DO IS I'LL GO BACK TO

1 THE -- WE'VE SEEN THIS SLIDE BEFORE -- THIS IS A
2 FAIRLY TYPICAL SDRAM SYSTEM TOPOLOGY THAT WE TALKED
3 ABOUT LAST THURSDAY IN THE TUTORIAL, AND TYPICALLY
4 THE INDIVIDUAL -- THIS IS SDRAMS, THIS IS CLOSELY
5 ANALOGOUS TO A DDR SDRAM SYSTEM, THAT TYPICALLY
6 THESE CHIPS ARE MOUNTED ON INDIVIDUAL CIRCUIT CARDS
7 THAT, TOGETHER, FORM MODULES.

8 AND, FOR EXAMPLE, THERE WILL BE PERHAPS
9 TWO CHIPS OR FOUR CHIPS OR EIGHT CHIPS OUTPUTTING
10 DATA IN PARALLEL TO SEPARATE SECTIONS OF THE DATA
11 BUS.

12 SO, FOR EXAMPLE, IF WE HAD FOUR CHIPS ON
13 A MODULE THAT WERE CONFIGURED IN A BY EIGHT
14 CONFIGURATION, THAT IS, WITH EIGHT DATA I/O LINES
15 FOR EACH CHIP, THAT THOSE CHIPS WOULD BE OPERATED
16 SUBSTANTIALLY SIMULTANEOUSLY TO OUTPUT A 32-BIT
17 WORD, OR 32 BITS IN PARALLEL AT A TIME.

18 THE BURST LENGTH, WHICH, AS WE'VE ALREADY
19 DISCUSSED, CAN BE PROGRAMMED IN THE MODE REGISTER,
20 SPECIFIES THE -- IN THE ABSENCE OF ANY OTHER
21 COMMANDS, IT BASICALLY SAYS HOW MANY BITS WILL COME
22 OUT SERIALLY ON EACH PIN.

23 AND THE TOTAL AMOUNT OF DATA, WHICH IS
24 RETRIEVED FROM EACH DEVICE, OR EACH SDRAM CHIP
25 HERE, DEPENDS NOT ONLY ON THE NUMBER OF BITS THAT

1 WOULD BE OUTPUT SERIALY ON EACH PIN, BUT IT ALSO
2 DEPENDS ON THE NUMBER OF DATA I/O PINS ON THE BUS.

3 SO THE BURST SIZE, OR THE BURST LENGTH,
4 DOES NOT SPECIFY THE TOTAL AMOUNT OF DATA, OR DOES
5 NOT EVEN REPRESENT THE TOTAL AMOUNT OF DATA WHICH
6 IS TO BE OUTPUT IN RESPONSE TO A READ COMMAND.

7 THE SECOND THING IS THAT -- OR THE SECOND
8 POINT ON THIS ISSUE THAT I WANT TO RAISE IS THAT
9 THE MEMORY CONTROLLER, WHEN IT IS ASKING FOR DATA,
10 IS BASICALLY -- BASICALLY IT WILL BE ASKING FOR TWO
11 OR FOUR OR FIVE OR EIGHT SORT OF 32-BIT WORDS, IN
12 THIS CASE OF DATA FROM A MEMORY MODULE, AND THE
13 MEMORY CONTROLLER DOES NOT CARE HOW MANY BITS ARE
14 RETRIEVED FROM EACH PIN, OR SORRY, IT DOES CARE HOW
15 MANY BITS ARE RETRIEVED FROM EACH PIN.

16 BUT IT DOESN'T CARE HOW MANY MEMORY CHIPS
17 ARE RETRIEVED FROM EACH MEMORY CHIP ON THE MODULE.

18 THAT IS, IF A MEMORY CONTROLLER SENDS AN
19 ACTIVATE COMMAND AND THEN A READ COMMAND TO, SAY,
20 BANK 0, OR THE FIRST MEMORY MODULE THERE, WHAT IT
21 CARES ABOUT -- AND I'LL ASSUME HERE THAT IT'S NOT
22 SENDING ANY OTHER COMMANDS -- IS THAT IT WANTS TO
23 GET FOUR, FOR A BURST LENGTH OF FOUR, IT WANTS TO
24 GET FOUR 32-BIT CHUNKS OF DATA IN PARALLEL OFF THAT
25 MODULE.

1 AND THE CONTROLLER DOESN'T CARE WHETHER
2 THERE ARE TWO CHIPS, EACH OF WHICH HAS 16 DATA I/O
3 LINES ON THAT MODULE, OR WHETHER THERE ARE FOUR
4 CHIPS, EACH OF WHICH HAS EIGHT DATA LINES ON A
5 CHIP, OR WHETHER IT HAS EIGHT CHIPS ON THAT MODULE,
6 EACH OF WHICH HAS FOUR DATA LINES.

7 IN EACH CASE, IN EACH CASE IT'S GETTING
8 CHUNKS OF 32-BIT WORDS IN PARALLEL.

9 SO THAT THE MEMORY CONTROLLER DOESN'T
10 CARE HOW MUCH DATA, AND IN GENERAL DOESN'T KNOW HOW
11 MUCH DATA, IT'S GETTING FROM ANY INDIVIDUAL CHIP.
12 ALL IT KNOWS, OR ALL IT WOULD KNOW IN THAT
13 CIRCUMSTANCE IS HOW MUCH DATA IT'S GETTING FROM THE
14 MODULE AS A WHOLE.

15 AND MR. MURPHY IN HIS DEPOSITION AGREED
16 WITH US, AND BASICALLY MR. MURPHY SAID, AFTER
17 BASICALLY I'D GONE THROUGH THIS KIND OF AN
18 EXPLANATION, WAS THAT THE CONTROLLER KNOWS HOW MANY
19 BITS TO OUTPUT, HOW MANY BITS SHOULD BE OUTPUT PER
20 MODULE, AND HE AGREED WITH THAT.

21 AND THE CONTROLLER DOES NOT NECESSARILY
22 KNOW OR CARE HOW MANY BITS ARE OUTPUT PER CHIP, AND
23 MR. MURPHY AGREED THAT THE CONTROLLER, THAT HE
24 DIDN'T THINK THE CONTROLLER CARED HOW MANY BITS
25 WERE OUTPUT PER CHIP.

1 SO THE BURST LENGTH THAT RAMBUS SAYS IS
2 EQUIVALENT TO BLOCK SIZE INFORMATION, IT DOES -- IS
3 NOT BLOCK SIZE INFORMATION BECAUSE IT DOES NOT
4 SPECIFY THE TOTAL AMOUNT OF DATA THAT IS TO BE
5 OUTPUT FROM A CHIP.

6 SECOND, AND THIS IS ALSO A SLIDE THAT
7 YOUR HONOR HAS SEEN BEFORE, LAST THURSDAY, BUT JUST
8 TO REVIEW BRIEFLY, THAT IN ORDER TO RETRIEVE DATA
9 FROM A CHIP, FIRST WHAT YOU HAVE TO DO IS YOU HAVE
10 TO SEND AN ACTIVATE COMMAND TO THE CHIP TO OPEN A
11 ROW, AND THEN, AT LEAST IN EITHER SDRAM OR DDR,
12 AFTER THAT YOU SEND A READ COMMAND WITH THE COLUMN
13 ADDRESS.

14 AND IN THE ABSENCE OF ANY FURTHER
15 COMMANDS, THE RESULT WILL BE THAT ON EACH PIN --
16 SORRY -- ON EACH PIN, THERE WILL BE FOUR DATA BITS
17 OUTPUT SERIALY FOR A BURST LENGTH OF FOUR.

18 AND I'VE BEEN CAREFUL TO SAY IN THE
19 TUTORIAL AND HERE THAT IN THE ABSENCE OF ANY
20 FURTHER COMMANDS, BECAUSE THE CONTROLLER CAN ISSUE
21 OTHER COMMANDS THAT CHANGE THE TOTAL AMOUNT OF DATA
22 THAT COMES OUT PER PIN AND, OF COURSE, CAN CHANGE
23 THE TOTAL AMOUNT OF DATA WHICH COMES OUT PER CHIP.

24 THE CONTROLLER IS NOT STUCK WITH GETTING
25 BITS OUT FOUR BITS AT A TIME ON A PIN.

1 OKAY. THERE ARE A NUMBER OF OTHER
2 SEQUENCES OF COMMANDS OR OPERATIONS THAT THE
3 CONTROLLER CAN DO IF IT WANTS, THAT IT IS CAPABLE
4 OF DOING THAT CHANGE THE NUMBER OF BITS THAT ARE
5 OUTPUT ON EACH PIN.

6 THIS IS JUST ANOTHER EXAMPLE, A SOMEWHAT
7 SIMPLIFIED PICTURE, AND THIS IS FROM TAYLOR EXHIBIT
8 66 WITH AN SDRAM, AND IT BASICALLY SHOWS THE SAME
9 INFORMATION THAT WAS ON THE PREVIOUS PAGE, EXCEPT
10 IT SHOWS IT IN A SOMEWHAT SIMPLIFIED FORM.

11 THERE IS AN ACTIVATE COMMAND, THEN THERE
12 IS A READ COMMAND, AND THEN AFTER, OR AT
13 APPROXIMATELY -- ON THE THIRD CLOCK CYCLE, BECAUSE
14 THIS IS A CAS LATENCY SYSTEM, YOU START GETTING THE
15 BITS OUT AND YOU ARE GET FOUR BITS IN BURST LENGTH
16 FOUR, FOUR BITS OUT SERIALY PER PIN.

17 NOW, ON THE OTHER HAND, IF THE
18 CONTROLLER -- AND BASICALLY THIS IS NOW A CAS
19 LATENCY 2 SYSTEM.

20 BUT IF THE CONTROLLER DOES AN ACTIVATE
21 COMMAND AND THEN DOES A READ COMMAND WITH THE
22 COLUMN ADDRESS, TWO CYCLES LATER THE BITS WILL
23 START COMING OUT FROM THAT READ COMMAND.

24 NOW, BUT IF THE CONTROLLER ON, IN THIS
25 CASE, THE NEXT CLOCK CYCLE ISSUES A SECOND READ

1 COMMAND WITH A, WITH A SECOND COLUMN ADDRESS, THE
2 THREE BITS THAT WOULD HAVE COME OUT IN RESPONSE TO
3 THE FIRST READ COMMAND DO NOT COME OUT ANYMORE.

4 OKAY. TWO CYCLES AFTER THE SECOND READ
5 COMMAND, THE BITS STARTING AT THE COLUMN ADDRESS
6 SPECIFIED WITH THE SECOND READ COMMAND ARE OUTPUT
7 ON EACH PIN.

8 SO IF THE CONTROLLER WANTS, FOR EXAMPLE,
9 FIVE BITS OUTPUT PER PIN, THEN IT CAN STACK -- IT
10 CAN BASICALLY PUT TWO READ COMMANDS TOGETHER IN
11 THIS WAY AND IT WILL GET FIVE BITS.

12 IF, FOR EXAMPLE, INSTEAD OF HAVING THE
13 SECOND READ COMMAND ONE CLOCK CYCLE AFTER THE FIRST
14 CLOCK CYCLE, IF WE HAD HAD THE SECOND READ COMMAND
15 TWO BITS, OR TWO CYCLES AFTER THE FIRST READ CYCLE,
16 OR THE FIRST READ COMMAND, THEN WE WOULD GET TWO
17 BITS OUTPUT ON EACH PIN IN RESPONSE TO THE FIRST
18 READ COMMAND, AND THE SECOND READ COMMAND WOULD
19 TERMINATE THAT FIRST READ AFTER TWO BITS.

20 AND IN THE ABSENCE OF ANY FURTHER
21 COMMANDS, IT WOULD THEN -- THERE WOULD BE FOUR BITS
22 OUTPUT IN RESPONSE TO THE SECOND READ COMMAND, AND
23 IN THIS, THIS SITUATION WHERE THERE ARE TWO CLOCK
24 CYCLES SEPARATED BETWEEN READ COMMANDS, YOU WOULD
25 GET A TOTAL OF SIX BITS OUT PER PIN.

1 THE COURT: SO WHAT?

2 MR. BROWN: HUM?

3 THE COURT: SO WHAT? WHY DOES THIS MAKE
4 A DIFFERENCE?

5 MR. BROWN: WELL, WHAT I'M SAYING IS THAT
6 THE -- WELL, WHY IT MAKES A DIFFERENCE IS THAT THE
7 BURST LENGTH, OKAY, IN RESPONSE TO THE FIRST READ
8 COMMAND, OKAY, THE BURST LENGTH IS IRRELEVANT TO
9 HOW MANY BITS COME OUT.

10 IT MAY SET A MAXIMUM NUMBER OF BITS THAT
11 CAN COME OUT IN RESPONSE TO THAT FIRST READ
12 COMMAND, OKAY, BUT DEPENDING ON WHAT THE CONTROLLER
13 DOES AFTER THAT AND DEPENDING ON HOW MANY BITS THE
14 CONTROLLER WANTS, OKAY, THE NUMBER OF BITS WHICH
15 ARE OUTPUT IN RESPONSE TO THE FIRST COMMAND IS NOT
16 EQUAL TO THE, TO THE BURST LENGTH.

17 AND UNDER THE, THE TENTATIVE RULING, THE
18 TENTATIVE CONSTRUCTION THAT, THAT THE COURT HAS,
19 THE BURST LENGTH DOES NOT SPECIFY OR INDICATE THE
20 NUMBER OF BITS TO BE TRANSFERRED ON THE BUS IN
21 RESPONSE TO -- IN A READ OPERATION.

22 OKAY. THE NUMBER OF BITS THAT CAN BE
23 TRANSFERRED ON THE BUS IN THIS WHOLE READ OPERATION
24 WITH TWO READ COMMANDS IS FIVE, WHICH HAS NOTHING
25 TO -- THERE'S NO NECESSARY RELATIONSHIP TO THE

1 BURST LENGTH.

2 IF YOU TAKE THE FIRST READ COMMAND AS THE
3 FIRST READ OPERATION, THEN YOU ONLY GET, IN THIS
4 SITUATION, ONE BIT OUT IN RESPONSE TO THAT READ, TO
5 THAT FIRST READ COMMAND, EVEN THOUGH THE BURST
6 LENGTH IS SET TO FOUR.

7 THIS IS A SOMEWHAT FURTHER -- THIS IS A
8 FURTHER EXAMPLE WHERE NOW THE CONTROLLER WANTS TEN
9 BITS OUT PER PIN, AND THIS IS PRESSING MY POWER
10 POINT SKILLS, BUT BASICALLY WE HAVE THREE READ
11 COMMANDS. THE FIRST TWO READ COMMANDS ARE SPACED
12 BY FOUR CLOCK CYCLES, AND THAT MEANS THAT IN
13 RESPONSE TO THE FIRST READ COMMAND, YOU DO GET FOUR
14 BITS OUT SERIALY PER PIN.

15 IN RESPONSE TO THE -- AND THEN -- BUT
16 THEN THERE'S A THIRD READ COMMAND, WHICH IS TWO
17 CLOCK CYCLES AFTER THE SECOND.

18 AS A RESULT, THE THIRD READ COMMAND
19 INTERRUPTS THE SECOND READ COMMAND AND ONLY TWO
20 BITS ARE OUTPUT IN RESPONSE TO THE, TO THE SECOND
21 READ COMMAND, BUT FOUR ARE OUTPUT IN RESPONSE TO
22 THE THIRD READ COMMAND.

23 AGAIN, IN THE MIDDLE HERE, WE HAVE A READ
24 OPERATION WHERE THE NUMBER OF BITS OUTPUT ON A PIN
25 IS NOT EQUAL TO THE PREPROGRAMMED BURST LENGTH OF

1 FOUR IN THIS EXAMPLE.

2 NOW, THERE'S ANOTHER CONTROL SIGNAL WHICH
3 I HAVE NOT YET EXPLICITLY, OR THAT WE HAVEN'T
4 DISCUSSED, AND IT'S A CONTROL SIGNAL WHICH IS
5 PRESENT ON BOTH READ AND WRITE OPERATIONS IN AN
6 SDRAM, AND THAT'S WHAT'S KNOWN AS A DATA MASS.

7 OKAY. IN ADDITION IN RAS, CAS, WRITE
8 ENABLE AND CHIP SELECT, AND THERE ARE -- IT IS
9 SHOWN DOWN HERE AS A DQM SIGNAL, AND THAT IS A
10 SIGNAL WHICH, UNDER -- THAT THE CONTROLLER CAN
11 ISSUE TO MASK A PARTICULAR BIT OR SET OF BITS.

12 THERE ARE ACTUALLY TWO MASK OPERATIONS
13 SHOWN HERE, ONE FOR A WRITE OPERATION AND ONE FOR A
14 READ OPERATION, AND I'LL DISCUSS THE ONE
15 PARTICULARLY FOR A READ OPERATION.

16 OVER AT THE LEFT-HAND SIDE OF THIS TIMING
17 DIAGRAM, WE'VE OPENED A ROW.

18 THEN THERE IS A READ COMMAND AND NOTHING
19 ELSE HAPPENS, SO WE GET FOUR BITS OUTPUT ON THE
20 DATA LINE.

21 THEN THERE IS A WRITE COMMAND, WHICH I'LL
22 IGNORE FOR JUST A MOMENT.

23 AND THEN FOLLOWING THAT WRITE COMMAND,
24 THERE IS YET ANOTHER READ COMMAND.

25 NOW -- THIS IS ALL, AGAIN, WITH A BURST

1 LENGTH SET AT FOUR.

2 TWO CYCLES AFTER THAT SECOND READ
3 COMMAND, THE COMMAND THAT'S CLOSEST TO THE RIGHT,
4 THE CONTROLLER IN THIS CASE, CAN ASSERT THE DQM, OR
5 THE DATA MASK SIGNAL.

6 NOW, WHAT THAT MEANS IN THAT CASE, AND
7 THE SIGNAL RISING RIGHT HERE IS WHERE IT IS SHOWING
8 THAT THE DATA MASK IS BEING ASSERTED -- TWO CYCLES
9 AFTER THE ASSERTION OF THAT DATA MASK, THE EFFECT
10 IS THAT IT SUPPRESSES THAT THIRD BIT OUTPUT IN THAT
11 SERIES OF FOUR.

12 SO, AGAIN, THE NUMBER OF BITS WHICH ARE
13 TRANSFERRED PER PIN IN THIS CASE IS NOT EQUAL TO
14 THE BURST LENGTH.

15 THAT IS, THE CONTROLLER, BY ASSERTING
16 THIS DATA MASK SIGNAL, CAN EFFECTIVELY PREVENT THE
17 OUTPUT OF THE THIRD BIT IN THAT SERIES.

18 THE COURT: THE FACT THAT IT COULD DO IT
19 DOESN'T MEAN THAT IT NECESSARILY DOESN'T INFRINGE,
20 DOES IT, OR MEET THE LIMITATION IF IT COULD MEET
21 THE LIMITATION?

22 MR. BROWN: IF IT COULD MEET THE
23 LIMITATION, THEN PERHAPS IT COULD INFRINGE.

24 WHAT I'M TRYING TO SHOW HERE IS THE BURST
25 LENGTH, WHICH IS PROGRAMMED INTO THE -- THAT IS

1 PROGRAMMED INTO THE REGISTER HAS NO NECESSARY
2 RELATIONSHIP TO THE NUMBER OF BITS WHICH ARE
3 OUTPUT.

4 EACH -- THE CONTROLLER BASICALLY, IT'S A
5 RARE -- IT WOULD BE A RARE SITUATION WHERE THE
6 CONTROLLER ALWAYS WANTS EXACTLY THE SAME NUMBER OF
7 BITS.

8 IT -- THERE ARE TIMES WHEN IT WANTS TWO
9 BITS, THERE ARE TIMES WHEN IT WANTS ONE BIT, THERE
10 ARE TIMES WHEN IT WANTS THREE BITS OR FOUR BITS OR
11 SOME OTHER NUMBER OF BITS, AND IT MAY NOT WANT THE
12 BITS FROM SEQUENTIAL COLUMN ADDRESSES, WHICH ARE
13 WHAT IS GENERATED INTERNALLY.

14 SO IT MAY -- THE CONTROLLER MAY WANT JUST
15 THE FIRST, SECOND AND FOURTH BITS, OKAY, AND NOT
16 WANT THE THIRD BIT.

17 SO WHAT IT DOES IN THIS CASE IS IT
18 ASSERTS THE DATA MASK SO THAT IT DOES NOT -- IT
19 CHOOSES NOT TO GET THE THIRD BIT.

20 OKAY. THE BURST LENGTH, WHICH IS SET IN
21 THE MODE REGISTER, IS JUST SET AS SORT OF A DEFAULT
22 OF THE NUMBER OF INTERNAL COLUMN ADDRESSES WHICH
23 ARE GENERATED IN THE CHIP AND HAS NOTHING, HAS NO
24 NECESSARY RELATION AND NO PARTICULAR RELATION TO
25 THE NUMBER OF BITS WHICH ARE ACTUALLY OUTPUT IN

1 RESPONSE TO A READ COMMAND OR IN RESPONSE TO A
2 SERIES OF READ COMMANDS.

3 THERE IS A SIMILAR DATA MASKING OPERATION
4 ON THE WRITE, ON THE WRITE OPERATION, WHICH WE HAVE
5 NOT TALKED ABOUT A WHOLE LOT, EXCEPT THAT WHEN
6 THERE IS A DATA MASK SIGNAL ASSERTED ON THE WRITE
7 OPERATION, WHICH IS WHAT IS SHOWN HERE, BASICALLY
8 IT PREVENTS THIS, THE THIRD BIT IN THAT SEQUENCE,
9 AT THE SAME TIME AS THE DATA MASK, FROM BEING
10 TRANSFERRED TO THE MEMORY CHIP.

11 THERE'S A SIMILAR KIND OF OPERATION, AND
12 I'M GOING TO TRY AND GO THROUGH THIS RELATIVELY
13 QUICKLY, IN DDR.

14 IN THE DDR SDRAM FOLLOWING AN ACTIVATE
15 COMMAND, AND THEN FOLLOWING -- AND THEN WITH A READ
16 COMMAND, THEN TWO CYCLES LATER IN A CAS LATENCY
17 SYSTEM, THERE WILL BE FOUR BITS OUTPUT IN THE
18 ABSENCE OF ANY FURTHER COMMANDS.

19 AND THIS IS JUST AN EXAMPLE OF BASICALLY
20 TWO BACK-TO-BACK COMMANDS, TWO BACK-TO-BACK READ
21 COMMANDS WHERE, WHICH ARE SPACED BY TWO CLOCK
22 CYCLES. TWO CLOCK CYCLES IS SUFFICIENT TO, IN THE
23 NORMAL SCHEME OF THINGS, TO OUTPUT FOUR BITS OF
24 DATA.

25 SO IN THIS READ OPERATION, THERE ARE TWO

1 READ COMMANDS, AND AS A RESULT, THERE ARE A TOTAL
2 OF EIGHT BITS OF DATA THAT ARE OUTPUT.

3 HOWEVER, IF THE SECOND READ COMMAND IS
4 ISSUED ONE CLOCK CYCLE AFTER THE FIRST READ
5 COMMAND, THEN THE SECOND READ COMMAND WILL
6 TERMINATE THE FIRST BURST READ AND ONLY TWO BITS
7 WILL BE OUTPUT IN RESPONSE TO THE FIRST READ
8 COMMAND, EVEN THOUGH THE BURST LENGTH IS SET TO
9 FOUR.

10 SO THE BURST LENGTH IS A CONVENIENCE, BUT
11 IT DOES NOT GOVERN HOW MANY BITS ARE OUTPUT IN
12 RESPONSE TO A READ COMMAND.

13 THERE ARE ALSO OTHER WAYS OF INTERRUPTING
14 THE BURST, AGAIN, UNDER THE CONTROL OF THE
15 CONTROLLER.

16 THIS IS A COMMAND THAT WE HAVE NOT SEEN
17 BEFORE, BUT IT IS AN ALTERNATE COMMAND WHICH CAN BE
18 USED IN EITHER THE SDRAM OR THE DDR SDRAM, AND THAT
19 IS PRECHARGE COMMAND.

20 AND THIS IS AN EXAMPLE OF WHERE -- AND WE
21 TALKED ABOUT PRECHARGING AND WHAT PRECHARGING DOES.
22 AS YOUR HONOR WILL RECALL, IT BASICALLY TAKES THE
23 DATA WHICH IS ON THE SENSE AMPLIFIERS AND READS IT
24 BACK INTO THE CELLS AND PREPARES THE BIT LINES AND
25 THE SENSE AMPLIFIERS FOR THE NEXT READ OPERATION OR

1 THE NEXT WRITE OPERATION.

2 AND IN THIS CASE, THERE IS A PRECHARGE
3 COMMAND GIVEN ONE CYCLE AFTER THE READ COMMAND AND,
4 AS A RESULT, THE BURST IS INTERRUPTED AFTER TWO
5 BITS EVEN THOUGH THE, THE BURST LENGTH IS SET TO
6 FOUR IN THAT CASE.

7 THERE'S ALSO A BURST STOP COMMAND IN BOTH
8 SDRAM AND DDR THAT -- IF THE CONTROLLER ISSUES IT,
9 IF IT ONLY WANTS TWO BITS, THEN WHAT IT DOES IS IT
10 CAN ISSUE A BURST STOP COMMAND AND THE BURST
11 TERMINATES. YOU ONLY GET TWO BITS OUT, OUTPUT FROM
12 THE CHIP IN RESPONSE TO THE READ COMMAND EVEN
13 THOUGH, AGAIN, THE BURST LENGTH IS SET TO FOUR.

14 THE COURT: HOW WOULD YOU DEFINE "BURST"
15 OR "BURST LENGTH"?

16 MR. BROWN: HOW WOULD I DEFINE THE BURST?

17 THE COURT: IF I WERE TO ASK YOU, "WHAT
18 DOES THAT TERM MEAN" --

19 MR. BROWN: THE BURST LENGTH IS THE --
20 SORRY. REMEMBER, BACK ON THURSDAY, THERE WAS A
21 MODE REGISTER ON THE SDRAM AND ON THE DDR.

22 THE COURT: RIGHT.

23 MR. BROWN: AND THERE WAS A CODE IN
24 THERE. THERE ARE THREE, THREE BITS IN THE MODE
25 REGISTER THAT SPECIFY WHAT THE BURST LENGTH IS,

1 OKAY, THAT WILL SET IT TO EITHER TWO OR FOUR OR
2 EIGHT.

3 OKAY. AND THAT IS THE, THE TWO OR FOUR
4 OR EIGHT IS THE NUMBER OF BITS THAT, IN THE ABSENCE
5 OF ANYTHING ELSE, ANY OTHER ACTION TAKEN BY THE
6 CONTROLLER, THAT IS THE NUMBER OF BITS THAT WILL
7 COME OUT IN RESPONSE TO A READ COMMAND.

8 AND THAT IS -- IT'S THAT BURST LENGTH
9 WHICH IS PROGRAMMED INTO THE CONTROLLER THAT IS
10 ACCUSED OF, THAT RAMBUS ACCUSES OF BEING THE SAME
11 AS BLOCK SIZE INFORMATION IN THEIR CLAIMS.

12 AND THAT IS THE SOLE FEATURE OF THE, THE
13 SOLE FEATURE IN THE ACCUSED PRODUCTS THAT RAMBUS
14 HAS IDENTIFIED AS BEING EQUIVALENT TO OR THE SAME
15 AS THE BLOCK SIZE INFORMATION IN THEIR CLAIMS.

16 THE COURT: OKAY.

17 MR. BROWN: AND BASICALLY MR. MURPHY
18 AGREED IN HIS DEPOSITION, AND I'VE GOT THE PAGES
19 CITED HERE, WE DID FILE THIS YESTERDAY AND I HAVE
20 EXTRA COPIES OF THE DEPOSITION DESIGNATIONS FOR
21 YOU, YOUR HONOR.

22 AND IN PARTICULAR ON THIS ISSUE, I THINK
23 THAT THESE ARE THE, THE RELEVANT PAGES ARE 136,
24 LINE 18 TO 142, LINE 10; AND 143 LINE 89 TO 145,
25 LINE 17.

1 BUT IN PARTICULAR, ON PART OF THIS AT
2 PAGE 141, MR. MURPHY AGREED THAT THE CONTROLLER IS
3 WHAT CONTROLS THE NUMBER OF BITS WHICH ARE OUTPUT
4 IN RESPONSE TO A READ COMMAND. IT'S NOT THE BURST
5 LENGTH.

6 THE CONTROLLER IS NOT TIED TO GETTING
7 BITS FROM THE MEMORY IN CHUNKS EQUAL TO THE BURST
8 LENGTH. BASICALLY THE CONTROLLER MAKES THE
9 DECISIONS, AND IF THE CONTROLLER WANTS FIVE BITS,
10 IT CAN DO THAT. IF IT WANTS THREE BITS, IT CAN DO
11 THAT.

12 AND EVENTUALLY, THERE WERE -- THE RECORD
13 IS NOT AS CLEAN AS I WOULD LIKE, BUT THE CONTROLLER
14 CAN PICK ANY NUMBER OF BITS TO COME OUT PER PIN,
15 REGARDLESS OF WHETHER THE BURST LENGTH IS SET TO
16 TWO OR FOUR OR EIGHT.

17 AND MR. MURPHY AGREED THAT THE NUMBER OF
18 BITS OF INFORMATION COMING FROM THE DEVICE IS A
19 CONTINUOUS -- HE SAYS A CONTINUOUS STREAM OF
20 INFORMATION OF WHATEVER NUMBER OF BITS THAT THE
21 CONTROLLER WISHES TO GET.

22 AND ACTUALLY, HE ALSO AGREED THAT IT IS
23 NOT NECESSARILY A CONTINUOUS, A CONTINUOUS STREAM
24 BECAUSE OF THE USE OF THE DATA MASKING OPERATION,
25 THAT THE CONTROLLER, IF IT CHOOSES, CAN ISSUE A

1 DATA MASK WHICH INTERRUPTS THAT STREAM OR CAUSES
2 THE, THE STREAM OF DATA TO BE DISCONTINUOUS.

3 SO FOR THOSE REASONS -- BASICALLY THE
4 BLOCK SIZE, OR WHAT RAMBUS IDENTIFIES AS BLOCK SIZE
5 INFORMATION DOES NOT SPECIFY THE TOTAL AMOUNT OF
6 DATA THAT IS TO BE TRANSFERRED ON THE BUS DURING A
7 MEMORY READ OR WRITE OPERATION FOR AT LEAST TWO
8 REASONS.

9 ONE, THE BURST LENGTH THAT IS SET IN THE
10 MODE REGISTER DOES NOT SPECIFY THE TOTAL AMOUNT OF
11 DATA WHICH IS OUTPUT PER CHIP BECAUSE OF THE NUMBER
12 OF -- THE AMOUNT OF DATA WHICH IS OUTPUT PER CHIP
13 DEPENDS ON THE NUMBER OF DATA I/O LINES ON THAT
14 PARTICULAR CHIP IN ADDITION TO THE BURST LENGTH, OR
15 AT LEAST, THAT'S THE MAXIMUM THAT THE, THAT THE
16 CHIP CAN OUTPUT IN RESPONSE TO ONE READ COMMAND.

17 IN ADDITION, THOUGH, THE BURST LENGTH
18 THAT IS SET IN THE MODE REGISTER HAS NO NECESSARY
19 RELATIONSHIP TO THE NUMBER OF BITS THAT ARE OUTPUT
20 IN RESPONSE TO, DURING A READ OPERATION. THAT'S
21 ENTIRELY UNDER THE CONTROL OF THE CONTROLLER AND
22 THE IDENTIFIER IN THE SEQUENCE IN THE COMMAND THAT
23 IT ISSUES TO THE MEMORY CHIPS.

24 THE COURT: OKAY. THANK YOU.

25 MR. BROWN: OKAY.

1 MR. DETRE: WELL, YOUR HONOR, I'D LIKE TO
2 TAKE MR. BROWN'S TWO POINTS IN ORDER.

3 FIRST WITH RESPECT TO MR. BROWN'S POINT
4 ABOUT THE TOTAL AMOUNT OF DATA, MR. BROWN SAID THAT
5 THE BURST LENGTH IN THE ACCUSED DEVICES DON'T
6 REPRESENT A TOTAL AMOUNT OF DATA BECAUSE IT DEPENDS
7 ON THE NUMBER OF DATA I/O LINES OR OUTPUT PINS,
8 DATA PINS ON THE DEVICE.

9 WELL, AS WE'VE DISCUSSED TO SOME EXTENT
10 IN OUR BRIEFING, ANY REASONABLE IDEA OF BEING
11 REPRESENTATIVE, REPRESENTATIVE OF THE TOTAL AMOUNT
12 OF DATA OR SPECIFYING A TOTAL AMOUNT OF DATA WOULD
13 BE SATISFIED BECAUSE A MEMORY DEVICE HAS A FIXED
14 NUMBER OF DATA I/O LINES.

15 AND SO, FOR EXAMPLE, IF IT'S A BY EIGHT
16 PART, THAT MEANS IT HAS EIGHT DATA PINS, AND IF THE
17 BURST LENGTH IS SET TO FOUR, THEN IN THE NORMAL
18 COURSE -- AND I'LL GET TO MR. BROWN'S SECOND
19 ARGUMENT IN A BIT -- BUT IN THE NORMAL COURSE,
20 UNLESS INTERRUPTED BY ANOTHER COMMAND, IT WILL
21 OUTPUT 32 BITS, FOUR BITS PER PIN, FOUR BITS FOR
22 EACH OF THE EIGHT PINS.

23 NOW, MR. BROWN WENT ON TO TALK ABOUT
24 MODULES AND HOW, WHEN A CONTROLLER SENDS A READ
25 REQUEST TO A MODULE, IT'LL EXPECT TO GET DATA BACK

1 FROM EACH OF THE MEMORY CHIPS IN THAT MODULE.

2 I DON'T THINK THAT MR. BROWN EXPLAINED
3 HOW THIS IS IN ANY WAY RELEVANT TO THE CLAIMS THAT
4 ARE AT ISSUE HERE.

5 IF WE COULD PULL UP, JUST FOR AN EXAMPLE,
6 ONE OF THE CLAIMS THAT INVOLVE BLOCK SIZE
7 INFORMATION.

8 HAVE YOU GOT THE '918 PATENT? AND IF WE
9 COULD GO TO CLAIM 18. I'M SORRY. I DON'T HAVE THE
10 PAGE NUMBER HERE, BUT IT'S -- IT'S PAGE 30, AND
11 IT'S ON THE RIGHT-HAND COLUMN, CLAIM 18. THERE WE
12 GO.

13 THIS REFERS TO A METHOD OF OPERATION OF A
14 SYNCHRONOUS MEMORY DEVICE.

15 CLAIM 18 OF THE '918 PATENT, AND ALL OF
16 THE OTHER CLAIMS THAT INVOLVE BLOCK SIZE
17 INFORMATION, ARE ON A DEVICE BY DEVICE BASIS.
18 WE'RE TALKING ABOUT THE INDIVIDUAL MEMORY CHIPS,
19 NOT THE MODULES.

20 AND WHEN A CONTROLLER SENDS A READ
21 REQUEST AND IT GOES TO THE MODULE, THAT READ
22 REQUEST THEN GETS TRANSLATED INTO A READ REQUEST
23 THAT GOES TO EACH OF THE INDIVIDUAL MEMORY CHIPS ON
24 THAT MODULE AND EACH OF THOSE INDIVIDUAL MEMORY
25 CHIPS WILL THEN RESPOND BY OUTPUTTING, FOR EACH

1 DATA PIN, THE NUMBER OF BITS SPECIFIED BY THE BURST
2 LENGTH.

3 MR. BROWN ALSO MADE THE POINT THAT THE
4 MEMORY CONTROLLER DOESN'T KNOW OR CARE HOW MANY --
5 HOW MUCH DATA WILL BE COMING BACK FROM EACH
6 INDIVIDUAL DEVICE.

7 WELL, AGAIN, IT'S NOT CLEAR TO ME, AGAIN,
8 HOW THAT'S RELEVANT BECAUSE THE BLOCK SIZE
9 INFORMATION IN RAMBUS'S CLAIMS RELATES TO EACH
10 SPECIFIC DEVICE AND NOT TO THE DESIRES OR KNOWLEDGE
11 OF THE MEMORY CONTROLLER.

12 BUT, IN FACT, IT'S NOT EVEN TRUE THAT THE
13 MEMORY CONTROLLER DOESN'T KNOW HOW MUCH DATA WILL
14 BE COMING BACK FROM EACH MEMORY DEVICE. IT DOES
15 KNOW.

16 THIS ARGUMENT WAS NOT ACTUALLY MADE IN
17 HYNIX'S BRIEFING, SO WE COULD NOT RESPOND IN OUR
18 BRIEFING, BUT WE DO HAVE A DATA SHEET OF A HYNIX
19 MODULE THAT I DOWNLOADED THE OTHER DAY FROM HYNIX'S
20 WEB SITE.

21 AND IF WE COULD PULL THAT UP, THE MODULE
22 DATA SHEET. MDS, I THINK YOU CALLED IT, THE MODULE
23 DATA SHEET. I THINK YOU CALLED IT MDS. NO, THE
24 MODULE DATA SHEET. I THINK YOU CALLED IT MDS. AH,
25 THERE WE GO.

1 THAT'S A DATA SHEET FOR A HYNIX
2 UNBUFFERED DDR SDRAM DIMM. DIMM STANDS FOR, I
3 BELIEVE, DUAL IN-LINE MEMORY MODULE, AND IT'S A
4 PARTICULAR KIND OF MODULE, AND THIS ONE IS FOR DDR
5 SDRAM IN PARTICULAR.

6 AND IF WE LOOK AT THE LAST PARAGRAPH IN
7 THE DESCRIPTION, IT NOTES THAT -- NO, NO, BACK
8 WHERE YOU WERE -- IN THE LAST PARAGRAPH IN THE
9 DESCRIPTION, IT NOTES THAT THIS PARTICULAR MODULE
10 INCORPORATES SOMETHING CALLED SERIAL PRESENCE
11 DETECT, AND THAT'S A LITTLE BIT OF NON-VOLATILE
12 MEMORY THAT'S ON THE MODULE SO THAT WHEN THE SYSTEM
13 POWERS UP, THE CONTROLLER CAN TELL WHAT KIND OF
14 MODULES IT HAS IN ITS MEMORY AND WHAT IT'S DEALING
15 WITH.

16 AND IT READS THE INFORMATION SERIALLY
17 FROM THE, FROM THIS LITTLE BIT OF NON-VOLATILE
18 MEMORY THERE, IN THIS CASE, 2,048-BIT EEPROM.

19 AND IF WE COULD GO TO, I BELIEVE IT'S THE
20 SECOND TO LAST PAGE WHICH DESCRIBES WHAT SORT OF
21 INFORMATION IS AVAILABLE TO THE CONTROLLER -- KEEP
22 GOING. IS THERE A FASTER WAY TO GET TO THE SECOND
23 TO LAST PAGE? THERE WE GO. STOP. AND IF YOU
24 COULD BLOW UP, I BELIEVE IT'S LINE 13 OF THESE, OF
25 THE INFORMATION THAT'S CONTAINED IN THAT SERIAL

1 PRESENCE DETECT.

2 IT TALKS ABOUT THE PRIMARY DDR SDRAM
3 WIDTH, AND IT SAYS IT'S BY 8, WHICH IS PROVIDING
4 INFORMATION TO THE CONTROLLER ABOUT EXACTLY WHAT
5 KIND OF CHIPS IT'S DEALING WITH, AND IN THIS CASE,
6 FOR THIS PARTICULAR MODULE, THEY'RE BY EIGHT CHIPS.
7 THEY EACH HAVE EIGHT DATA PINS.

8 SO, AGAIN, I DON'T THINK THE MODULES ARE
9 RELEVANT.

10 TO THE EXTENT THEY ARE, THE CONTROLLER
11 KNOWS EXACTLY WHAT IT'S DEALING WITH AND KNOWS HOW
12 MUCH DATA IT'S GOING TO GET BACK FROM EACH CHIP.

13 MR. BROWN'S -- THIS CAN GO.

14 MR. BROWN'S SECOND POINT WAS ABOUT THE
15 POSSIBILITY OF ISSUING OTHER COMMANDS TO INTERRUPT
16 A BURST IN PROGRESS OR TO MASK IT.

17 WELL, I HAVE A FEW POINTS TO MAKE IN
18 RESPONSE TO THAT.

19 FIRST, THE -- HYNIX'S CONSTRUCTION,
20 RAMBUS'S PROPOSED CONSTRUCTION, AND THE COURT'S
21 TENTATIVE CONSTRUCTION ALL TALK ABOUT THE AMOUNT OF
22 DATA TO BE TRANSFERRED.

23 "TO BE TRANSFERRED" MUST HAVE SOME
24 DIFFERENT MEANING FROM WHAT ACTUALLY IS
25 TRANSFERRED.

1 "TO BE TRANSFERRED" IS THE AMOUNT THAT
2 YOU WOULD TRANSFER IN THE NORMAL COURSE IF YOU DID
3 NOT THEN ISSUE SOME OTHER COMMAND TO CUT OFF THAT
4 BURST.

5 SECOND, MR. BROWN, I THINK, OVERSTATED
6 THE AMOUNT OF DISCRETION HERE BASICALLY ON THE PART
7 OF THE CONTROLLER IN VARIOUS RESPECTS, AND THESE
8 ARE RELATIVELY MINOR POINTS, BUT I DO WANT TO JUST
9 MENTION QUICKLY THAT THE DATA MASKING OPERATION
10 THAT MR. BROWN WAS TALKING ABOUT, WHICH IS FOR BOTH
11 READS AND WRITES IN SDRAMs, IS ONLY FOR WRITES IN
12 DDR SDRAMs.

13 AND THAT'S MADE FAIRLY CLEAR IN HYNIX'S
14 DDR SDRAM DATA SHEET, AND THIS IS EXHIBIT 68 TO
15 MR. TAYLOR'S, ONE OF MR. TAYLOR'S DECLARATIONS.

16 IT'S AT PAGE 32 OF THAT DATA SHEET WHERE
17 HE TALKS ABOUT DATA MASKING WRITE, AND IT SAYS, "DM
18 COMMAND MASKS BURST WRITE DATA WITH REFERENCE TO
19 DATA STROBE SIGNAL AND IT IS NOT RELATED WITH READ
20 DATA."

21 IT'S NOT PERFECT ENGLISH, BUT IT MEANS
22 THAT IT'S NOT AVAILABLE FOR READ COMMANDS FOR DDR
23 SDRAMs, AND MR. TAYLOR TESTIFIED TO THAT IN HIS
24 DEPOSITION.

25 MR. BROWN ALSO TALKED ABOUT THE PRECHARGE

1 COMMAND CUTTING OFF A READ BURST, BUT AS THE -- IN
2 BOTH SDRAMs AND DDR COMMANDS, THE PRECHARGE COMMAND
3 CAN -- MR. BROWN TALKED ABOUT THE PRECHARGE COMMAND
4 AND ALSO THE BURST STOP COMMAND.

5 BUT IN BOTH DDR SDRAMs AND SDRAMs,
6 INTERRUPTING BURSTS, WHETHER WITH A PRECHARGE OR A
7 BURST STOP OR ANOTHER READ OR WRITE COMMAND IS NOT
8 AVAILABLE FOR A READ WITH AUTO PRECHARGE.

9 AND IF WE COULD PULL UP THE SDRAM DEVICE
10 OPERATION DOCUMENT? AND GO TO PAGE 7, AND BLOW UP
11 THE TOP TEXT.

12 AT THE BOTTOM, IT NOTES HERE, "A READ OR
13 WRITE COMMAND WITH AUTO PRECHARGE CANNOT BE
14 TERMINATED BY READ, WRITE, PRECHARGE AND BURST
15 STOP."

16 SO AT LEAST FOR THAT CLASS OF READ
17 COMMAND, YOU CAN'T CHANGE THE BURST LENGTH ONCE
18 YOU'VE ISSUED THE COMMAND IN THE WAY, IN SOME OF
19 THE WAYS THAT MR. BROWN DESCRIBED.

20 BUT MR. BROWN ALSO SAID THAT IT WAS, YOU
21 KNOW, "A FAIR SITUATION" I THINK ARE THE WORDS HE
22 USED, WHEN A CONTROLLER WOULD ALWAYS WANT THE SAME
23 NUMBER OF BITS.

24 I DON'T THINK THAT THERE'S ANY EVIDENCE
25 IN THE RECORD TO SUPPORT THAT STATEMENT, AND I ALSO

1 DON'T THINK IT'S ACCURATE.

2 IN THE PROCESSORS THAT ARE IN USE TODAY,
3 PRIMARILY BY AMD AND INTEL, THE PROCESSORS CONTAIN
4 A CACHE, AND THERE'S A CERTAIN LENGTH OF CACHE
5 LINE, AND TO EFFICIENTLY FILL THE CACHE LINE WITH
6 DATA, A CERTAIN BURST LENGTH IS OPTIMAL.

7 AND IN FACT, THERE'S NO EVIDENCE IN THE
8 RECORD ABOUT THIS EITHER, BUT IN FACT, IT IS THE
9 CASE THAT DIFFERENT BURST LENGTHS OF FOUR AND EIGHT
10 WERE SPECIFICALLY DEMANDED BY AMD AND INTEL
11 SPECIFICALLY BECAUSE THEY WANTED THOSE OPTIMAL
12 LENGTHS TO FILL THE DIFFERENT SIZES OF THEIR CACHE
13 LINES IN THEIR PROCESSORS.

14 THE MAIN POINT I WANT TO MAKE, THOUGH, IS
15 THAT EVEN THOUGH MR. BROWN OVERSTATES THE
16 SITUATIONS IN WHICH YOU CAN INTERRUPT THESE BURSTS
17 OR CUT THEM OFF OR CHANGE THEM, ALL THAT'S REALLY
18 REQUIRED FOR INFRINGEMENT, AS WE POINTED OUT IN OUR
19 PAPERS AND WE CITED CASES, IS THAT THE DEVICES BE
20 REASONABLY CAPABLE OF PERFORMING IN AN INFRINGING
21 MANNER.

22 AND THE DATA SHEETS SHOW THAT THEY ARE,
23 AND MR. BROWN HIMSELF SHOWED AN EXAMPLE, THE TIMING
24 DIAGRAM ON A DATA SHEET WHERE IT SHOWED A COMPLETE
25 BURST. THAT'S HOW HYNIX REFERS TO BURSTS THAT ARE

1 NOT INTERRUPTED IN THEIR PAPERS.

2 THIS TIMING DIAGRAM THAT WE HAVE RIGHT
3 HERE ON THE SCREEN SHOWS THAT. THE BURST LENGTH IS
4 FOUR AND FOUR BITS OF DATA ARE COMING OUT.

5 AND MR. TAYLOR, AT HIS DEPOSITION,
6 TESTIFIED TO THAT.

7 AND IF WE COULD PULL UP GRAPHIC NUMBER
8 64, WHICH IS A COUPLE OF QUOTES.

9 AND THE QUESTION WAS, "YOU GO ON IN YOUR
10 DECLARATION TO TALK ABOUT THE POSSIBILITY IN THE
11 HYNIX DEVICES OF INTERRUPTING BURSTS OF DATA WITH A
12 BURST STOP COMMAND OR WITH A READ OR WRITE COMMAND;
13 CORRECT?"

14 "ANSWER: A NEW LOAD OF DATA OR A NEW
15 READ COMMAND, YES."

16 "QUESTION: OKAY. IS IT POSSIBLE FOR A
17 USER TO OPERATE HYNIX'S DEVICES WITHOUT
18 INTERRUPTING BURSTS OF DATA?"

19 "ANSWER: YES."

20 SIMILAR ANSWER WITH RESPECT TO MASKING
21 DATA.

22 "QUESTION: IS IT POSSIBLE FOR A USER TO
23 OPERATE HYNIX'S DEVICES WITHOUT MASKING DATA ON
24 WRITES?"

25 "ANSWER: YES."

1 WE WERE SPECIFICALLY TALKING ONLY ABOUT
2 WRITE DATA HERE BECAUSE MR. TAYLOR HAD TESTIFIED
3 THAT THAT WAS ONLY AVAILABLE ON WRITES. I BELIEVE
4 HE WAS THINKING OF DDR SDRAMs.

5 SO CLEARLY THE DEVICES ARE REASONABLY
6 CAPABLE OF PERFORMING IN AN INFRINGING MANNER;
7 THEREFORE, THEY INFRINGE.

8 THE COURT: OKAY. SHALL WE MOVE ON?

9 MR. BROWN: SURE. AND --

10 THE COURT: I DO WANT TO -- I SHOULD
11 MENTION, WITH RESPECT TO RAMBUS'S MOTION, I DO WANT
12 TO TALK ABOUT THE ONE THAT DEALS WITH A READ
13 REQUEST.

14 MR. BROWN: WOULD YOU LIKE TO HEAR THAT
15 NEXT?

16 THE COURT: SURE, WHY DON'T WE DO THAT
17 NEXT?

18 MR. DETRE: SHOULD I GO FIRST ON RAMBUS'S
19 MOTION?

20 THE COURT: SURE, SINCE YOU'RE THE MOVING
21 PAPER, OR YOU'RE THE MOVING PARTY.

22 MR. DETRE: OKAY. WITH RESPECT TO READ
23 REQUEST, WE HAVE AN AGREED CONSTRUCTION OF THE
24 TERM. IT WAS THE CONSTRUCTION THAT WAS PROVIDED BY
25 THE FEDERAL CIRCUIT.

1 AND IF WE COULD PULL UP NUMBER 66.

2 THIS IS WHAT THE FEDERAL CIRCUIT SAID:

3 "FROM THE CORRECT PERSPECTIVE OF ONE OF SKILL IN
4 THE ART AT THE TIME OF INVENTION, THE TERM 'READ
5 REQUEST' MEANS A SERIES OF BITS USED TO REQUEST A
6 READ OF DATA FROM A MEMORY DEVICE WHERE THE REQUEST
7 IDENTIFIES WHAT TYPE OF READ TO PERFORM."

8 THE COURT: IS A READ REQUEST JUST A TYPE
9 OF OPERATION CODE?

10 MR. DETRE: WELL, I THINK IT IS, YES,
11 YOUR HONOR. I MEAN, I THINK BASICALLY, BASICALLY A
12 READ REQUEST IS -- CAN BE CONSIDERED AN OPERATION
13 CODE USED TO REQUEST A READ OF DATA.

14 THE COURT: AND DOESN'T REFERENCE TO
15 SERIES OF BITS SUGGEST A PACKET PROTOCOL?

16 MR. DETRE: NO, I DON'T THINK IT DOES,
17 YOUR HONOR.

18 HYNIX ARGUED THAT "SERIES OF BITS" DOES
19 REFLECT A PACKET PROTOCOL BECAUSE THOSE BITS NEED
20 TO -- THAT SERIES REPRESENTS A TIME SERIES AND
21 THOSE BITS HAVE TO BE RECEIVED OVER MULTIPLE CLOCK
22 CYCLES AS IN RAMBUS'S PACKETS, REQUEST PACKETS IN
23 THE PREFERRED EMBODIMENT.

24 BUT IF WE ACTUALLY LOOK AT WHAT THE
25 FEDERAL CIRCUIT WAS LOOKING AT WHEN THEY WERE

1 LOOKING AT THE READ REQUEST, THEY WERE, THEY WERE
2 GUIDED BY THE SPECIFICATION -- THE EXAMPLES IN THE
3 SPECIFICATION, WHICH -- AND THE PREFERRED
4 EMBODIMENT THERE DOES INVOLVE PACKETS.

5 BUT THEY WERE -- I DON'T THINK THEY WERE
6 IN ANY WAY TRYING TO RESTRICT RAMBUS TO THOSE, TO
7 PACKETS.

8 AND, IN FACT, WHAT THEY IDENTIFIED WITH
9 THE SERIES OF BITS IN THE PREFERRED EMBODIMENT WAS
10 JUST ONE LITTLE PIECE OF ONE PACKET, FOUR BITS THAT
11 ARE RECEIVED IN PARALLEL.

12 THEY'RE NOT A PACKET. THEY'RE JUST SOME
13 BITS WHICH, IN THE PREFERRED EMBODIMENT WHICH DOES
14 USE PACKETS, IS CONTAINED IN THE PACKET.

15 BUT THERE'S ABSOLUTELY NOTHING IN THE, IN
16 THE CONSTRUCTION THAT THEY CAME UP WITH THAT
17 SUGGESTS A PACKET.

18 THE COURT: WOULD YOU DEFINE FOR ME AGAIN
19 A PACKET?

20 MR. DETRE: WELL, AS I SAID YESTERDAY, I
21 THINK THAT THE TERM "PACKET" IS A SOMEWHAT VAGUE
22 TERM.

23 BUT HYNIX SEEMS TO THINK, AT LEAST
24 SOMETIMES, SOMETIMES IT SAYS THAT A PACKET NEEDS TO
25 BE DEFINED EXACTLY AS A REQUEST PACKET IN THE

1 PREFERRED EMBODIMENT, AND SOMETIMES IT SEEMS TO
2 IDENTIFY IT AS THE DISTINGUISHING FEATURE OF THE
3 FACT THAT THERE IS SOME KIND OF PACKET PROTOCOL
4 THAT ALLOWS YOU TO DETERMINE WHAT INFORMATION, WHAT
5 KIND OF INFORMATION IS BEING TRANSMITTED TO THE
6 DEVICE AT A GIVEN TIME.

7 IF WE --

8 THE COURT: OKAY. YOU TOLD ME HOW HYNIX
9 WOULD DEFINE IT.

10 HOW WOULD YOU DEFINE IT?

11 MR. DETRE: WELL, I -- I'M NOT SURE THAT
12 THERE IS A, THAT THE TERM "PACKET" IS ALWAYS USED
13 CONSISTENTLY BY PEOPLE OF SKILL IN THE ART.

14 I DO THINK THAT WHEN PEOPLE REFER TO A
15 PACKET, THEY DO THINK OF SOME SORT OF A PROTOCOL
16 THAT ALLOWS IDENTIFICATION OF THE INFORMATION.

17 I DON'T THINK, AS HYNIX HAS SAID, THAT IT
18 NEEDS TO BE TRANSMITTED OVER MULTIPLE CLOCK CYCLES
19 OR VARIOUS OTHER SORTS OF LIMITATIONS THAT HAVE
20 BEEN LOADED ONTO THAT TERM.

21 THE COURT: DO THE PATENTS IN ANY WAY --
22 OR IS THERE ANY EVIDENCE THAT THE SPECIFICATION
23 WOULD SUGGEST TO ONE SKILLED IN THE ART THAT THE
24 OPERATION CODE COULD BE TRANSMITTED OTHER THAN IN A
25 PACKET?

1 MR. DETRE: WELL, I THINK -- I THINK SO,
2 YOUR HONOR. I THINK THE ENTIRETY OF THE
3 SPECIFICATION LAYS OUT MULTIPLE DISTINCT INVENTIONS
4 AS THE PATENT OFFICE FOUND AND AS THE FEDERAL
5 CIRCUIT HAS CONFIRMED.

6 AND ONE OF THOSE INVENTIONS DEALS WITH
7 TRANSMITTING A REQUEST IN THAT, IN THE SORT OF
8 PACKET FORMAT SHOWN IN THE PATENT.

9 BUT I DON'T THINK THERE'S ANYTHING IN THE
10 PATENT --

11 (CELL PHONE RINGING IN THE AUDIENCE.)

12 THE COURT: LET ME JUST MAKE SURE
13 EVERYBODY HAS TURNED OFF THEIR CELL PHONE.

14 MY RULE IS I DON'T LIKE IT THE FIRST
15 TIME. THE SECOND TIME YOU'RE OUT OF HERE. SO JUST
16 BEAR THAT IN MIND.

17 I DON'T MEAN TO BE MEAN, BUT IT IS A
18 PROBLEM AND I NEED TO MAKE SURE IT'S DEALT WITH.

19 OKAY. GO AHEAD.

20 MR. DETRE: I DON'T THINK THERE'S
21 ANYTHING IN THE PATENT TO SUGGEST THAT THE OTHER
22 DISTINCT INVENTIONS THAT ARE NOT ABOUT THE
23 PARTICULAR PACKETIZED PROTOCOL THAT SOME OF
24 RAMBUS'S CLAIMS ARE DIRECTED TOWARDS, I DON'T THINK
25 THERE'S ANYTHING IN THE PATENT TO SUGGEST THAT THE

1 OTHER DISTINCT INVENTIONS ARE RESTRICTED TO SENDING
2 AN OPERATION CODE OR A READ REQUEST OR COMMANDS IN
3 ANY PARTICULAR WAY.

4 A PERSON OF SKILL IN THE ART WOULD
5 UNDERSTAND THAT YOU COULD SEND THOSE REQUESTS IN
6 ANY WAY THAT, THAT -- BASICALLY IN ANY WAY KNOWN TO
7 PEOPLE OF SKILL IN THE ART AND USE THESE DISTINCT
8 INVENTIONS, LIKE MANY OF THE DISTINCT INVENTIONS
9 WE'RE TALKING ABOUT HERE.

10 ACCESS TIME REGISTERS, THERE'S NOTHING
11 ABOUT AN ACCESS TIME REGISTER THAT IS IN ANY WAY
12 RESTRICTED TO A PARTICULAR METHOD OF TRANSMITTING A
13 COMMAND.

14 BLOCK SIZE INFORMATION, AGAIN, NOTHING IN
15 THAT THAT SUGGESTS IN ANY WAY THAT IT'S RESTRICTED
16 TO A SPECIFIC WAY OF SENDING THE COMMAND TO THE
17 DEVICE.

18 I THINK WHAT -- WHEN WE'RE DEALING HERE
19 WITH AN APPLICATION, AN ORIGINAL APPLICATION THAT
20 LAID OUT MULTIPLE DISTINCT INVENTIONS, I THINK THAT
21 THE APPLICATION DESCRIBED IN SOME CASES IS BEING
22 USED IN COMBINATION.

23 NEVERTHELESS, IT CAN -- IT CANNOT BE
24 RESTRICTED TO JUST USING THOSE COMBINATIONS
25 ALTOGETHER OR THERE WOULD BE ONLY ONE INVENTION.

1 AND THE INVENTIONS THAT ARE DISTINCT FROM
2 THE PACKET, I DON'T THINK THERE'S ANYTHING IN THE
3 PATENT TO SUGGEST THAT THEY SHOULD BE IN ANY WAY
4 LIMITED TO OPERATION CODES SENT IN PACKETS.

5 I WOULD --

6 THE COURT: IS THERE ANY PARTICULAR
7 LANGUAGE, OR IS IT JUST WHAT SOMEONE SKILLED IN THE
8 ART WOULD KNOW AT THE TIME?

9 MR. DETRE: WELL, I THINK -- I THINK IT'S
10 BOTH. THE ORIGINAL APPLICATION, OF COURSE -- AND
11 IF WE'RE DISCUSSING HERE THE WRITTEN DESCRIPTION
12 REQUIREMENT, YOUR HONOR --

13 THE COURT: I THINK, IN ESSENCE, WE ARE.

14 MR. DETRE: OKAY. THE ORIGINAL WRITTEN
15 DESCRIPTION, OF COURSE, INCLUDES THE ORIGINAL
16 CLAIMS.

17 THE COURT: RIGHT.

18 MR. DETRE: AND THERE'S NOTHING IN THE
19 ORIGINAL CLAIMS THAT WOULD SUGGEST THAT ALL THE
20 CLAIMS ARE DIRECTED TO PACKETS OR A PARTICULAR FORM
21 OF SENDING OPERATION CODES IN PACKETS.

22 IF -- SOME OF THE ORIGINAL CLAIMS DID
23 DISCUSS PACKETS. OTHERS DID NOT.

24 I THINK PRETTY CLEARLY ONE OF ORDINARY
25 SKILL, LOOKING AT THAT WRITTEN DESCRIPTION,

1 INCLUDING THE MULTITUDE OF DISTINCT INVENTIONS
2 DESCRIBED IN THE SPECIFICATION, FOLLOWED BY THE
3 ORIGINAL CLAIMS, SOME OF WHICH DISCUSS PACKETS AND
4 SOME OF WHICH DON'T, WOULD UNDERSTAND THAT THE ONES
5 THAT DIDN'T WERE NOT RESTRICTED TO SENDING
6 OPERATION CODES IN THAT WAY.

7 THE COURT: THEY DON'T EXPRESSLY TALK
8 ABOUT A DIFFERENT WAY, DO THEY? THEY JUST DON'T
9 SAY ONE WAY OR THE OTHER?

10 MR. DETRE: THEY DON'T -- EXCUSE ME, YOUR
11 HONOR.

12 THEY DON'T EXPRESSLY TALK ABOUT A
13 DIFFERENT WAY.

14 BUT IT'S -- THERE ARE A COUPLE OF, I
15 THINK, PATENT LAW DOCTRINES THAT ARE VERY RELEVANT
16 HERE. ONE IS THAT CLAIMS NEED NOT BE LIMITED TO A
17 PREFERRED EMBODIMENT, EVEN IF THERE IS ONLY A
18 SINGLE EMBODIMENT.

19 AND THE FEDERAL CIRCUIT HAS STATED THAT
20 REPEATEDLY. FOR EXAMPLE, ONE OF THE CASES WE CITE
21 IN OUR PAPERS, TELEFLEX VERSUS FICOSA, 299 F.3D AT
22 1313 AT 1325 MAKES THAT POINT.

23 WELL, OF COURSE, IF A CLAIM NEED NOT BE
24 LIMITED TO A PREFERRED EMBODIMENT, EVEN IF THERE'S
25 ONLY A SINGLE EMBODIMENT, THAT DOESN'T -- IT

1 FOLLOWS THAT, ALTHOUGH THAT WAS A CLAIM
2 CONSTRUCTION CASE, OBVIOUSLY THE FEDERAL CIRCUIT
3 WAS NOT SAYING, "BUT IF YOU CLAIM MORE BROADLY THAN
4 A SINGLE EMBODIMENT, THEN YOU AUTOMATICALLY ARE NOT
5 IN COMPLIANCE WITH THE WRITTEN DESCRIPTION
6 REQUIREMENT."

7 THAT WOULDN'T MAKE SENSE. YOU'RE ALLOWED
8 TO CLAIM MORE BROADLY.

9 SECOND, PATENTS NEED NOT TEACH THAT WHICH
10 IS ALREADY KNOWN, AND A GOOD CITE FOR THAT IS
11 INTEGRA LIFESCIENCES I, LIMITED VERSUS MERCK, 331
12 F.3D 860 AT 868.

13 AND THERE ARE OTHER CASES THAT SUGGEST
14 THAT, IN FACT, A PATENT SHOULD NOT BELABOR WHAT IS
15 ALREADY KNOWN BECAUSE IT JUST WOULD MAKE PATENT
16 DOCUMENTS MUCH LONGER THAN THEY NEED TO BE.

17 THE KNOWLEDGE OF PEOPLE SKILLED IN THE
18 ART IS ASSUMED HERE, AND ESPECIALLY IN THIS SORT OF
19 CASE WHERE THERE ARE SO MANY DISTINCT INVENTIONS,
20 TO TAKE ONE OF THEM AND READ IT INTO THE OTHERS
21 WOULD NOT BE PROPER.

22 I'D LIKE TO ALSO PULL UP A QUOTE THAT I
23 THINK IS RELEVANT FROM JUDGE NEWMAN IN THE REIFFIN
24 VERSUS MICROSOFT CASE -- SLIDE NUMBER 68 -- IN
25 WHICH SHE SAID IN THE CONCURRING OPINION, "IT IS

1 STANDARD FOR APPLICANTS TO PROVIDE CLAIMS THAT VARY
2 IN SCOPE AND IN CONTENT, INCLUDING SOME ELEMENTS OF
3 A NOVEL DEVICE OR METHOD, AND OMITTING OTHERS.
4 CLAIMING AN INVENTION IN THIS MANNER DOES NOT RAISE
5 AN ISSUE OF COMPLIANCE WITH SECTION 112, PARAGRAPH
6 1," THE WRITTEN DESCRIPTION REQUIREMENT.

7 SO I THINK IT IS QUITE CLEAR THAT FOR
8 THOSE INVENTIONS THAT ARE NOT ABOUT PACKETS, FOR
9 THOSE INVENTIONS, THE KNOWLEDGE OF A PERSON OF
10 ORDINARY SKILL IS ASSUMED, AND THAT PERSON OF
11 ORDINARY SKILL WILL KNOW VARIOUS WAYS TO TRANSMIT
12 OPERATION CODES TO THE DEVICES.

13 THERE'S NOTHING IN THE PATENT -- THE
14 FEDERAL CIRCUIT, WHEN READING IN LIMITATIONS FROM
15 CERTAIN EMBODIMENTS, HAS REQUIRED AN UNAMBIGUOUS
16 DISCLOSURE IN THE PATENT THAT THIS IS THE ONLY WAY
17 TO PERFORM THIS PARTICULAR INVENTION.

18 THAT'S, FOR EXAMPLE, IN THE GENTRY
19 GALLERY CASE WHICH HAS, TO A LARGE EXTENT, BEEN
20 DISCREDITED TO THE EXTENT THAT HYNIX SAYS.

21 BUT TO THE EXTENT THAT IT'S STILL GOOD
22 LAW --

23 THE COURT: I DON'T THINK THEY REALLY
24 DISAGREE WITH YOU ON WHAT THAT CASE SAYS.

25 MR. DETRE: WELL, PERHAPS NOT AS

1 EVIDENCED BY THEIR REPLY BRIEF.

2 THE COURT: RIGHT.

3 MR. DETRE: ALTHOUGH IN THEIR REPLY
4 BRIEF, I THINK, AND IN SOME OF THEIR MOTIONS,
5 HYNIX, WHILE AGREEING THAT THE ESSENTIAL ELEMENT
6 TEST HAS BEEN DISCREDITED, STILL SEEMS TO BE URGING
7 THAT VARIOUS FEATURES IN RAMBUS'S SPECIFICATION ARE
8 AN ESSENTIAL ELEMENT AND, THEREFORE, MUST BE IN ALL
9 OF THE CLAIMS.

10 I DON'T THINK THAT CAN BE SQUARED WITH
11 THE VARIOUS RESTRICTION REQUIREMENTS ISSUED BY THE
12 PTO, WHICH SEPARATE OUT VARIOUS INVENTIONS.

13 THE NUMBER OF PATENTS THAT HAVE ISSUED
14 CLAIMING VARIOUS DIFFERENT INVENTIONS, THE
15 STATEMENT OF THE FEDERAL CIRCUIT THAT THERE ARE
16 MANY INVENTIONS DISCLOSED, ALL OF THAT SUGGESTS
17 THAT YOU'VE GOT A LARGE NUMBER OF DISTINCT
18 INVENTIONS, THE ONES THAT DO NOT SPECIFICALLY CALL
19 OUT SOME SORT OF A PACKETIZED PROTOCOL DO NOT, DO
20 NOT DEPEND ON IT AND A PERSON OF ORDINARY SKILL
21 WOULD UNDERSTAND THAT.

22 AND AGAIN, THE SPECIFICATION SIMPLY DOES
23 NOT NEED TO TEACH THAT WHICH IS ALREADY KNOWN.

24 IF WE COULD GO --

25 THE COURT: I DIDN'T MEAN TO STEER YOU

1 OFF OUR SUBJECT.

2 MR. DETRE: WELL, I THINK THAT WAS
3 PROBABLY AN IMPORTANT SUBJECT TO DISCUSS, YOUR
4 HONOR.

5 GOING BACK TO WHAT THE FEDERAL CIRCUIT
6 ACTUALLY LOOKED AT WHEN IT WAS CONSTRUING READ
7 REQUEST, IT DID LOOK AT THE PREFERRED EMBODIMENT IN
8 THE SPECIFICATION.

9 AND IF WE COULD PULL UP NUMBER 65.

10 AND IT LOOKED AT FIGURE 4 OF THE '918
11 PATENT, WHICH SHOWS A REQUEST PACKET.

12 BUT THE POINT OF DISPUTE BEFORE THE
13 FEDERAL CIRCUIT WAS THAT INFINEON WAS ARGUING THAT
14 A READ REQUEST REALLY HAS TO BE THIS WHOLE REQUEST
15 PACKET. IT HAS TO INCLUDE ALL THE THINGS, ALL OF
16 THE INFORMATION NECESSARY FOR A READ OPERATION, THE
17 ADDRESS, THE BLOCK SIZE AND SO FORTH.

18 AND RAMBUS WAS MAKING THE POINT, NO,
19 THAT'S NOT RIGHT. THE READ REQUEST IN THE
20 PREFERRED EMBODIMENT, THE READ REQUEST ONLY
21 CORRESPONDS TO THE FOUR BITS OF THE ACCESS TYPE,
22 AND THAT'S SHOWN AT THE TOP, ACCESS TYPE 0 TO 3.
23 THAT'S FOUR BITS, 0, 1, 2, 3.

24 THOSE BITS, WHILE IN THIS PARTICULAR
25 PREFERRED EMBODIMENT, ARE TRANSMITTED IN THE

1 PACKET. THERE'S NO REASON WHY FOUR BITS LIKE THAT
2 NEED TO BE TRANSMITTED IN THE PACKET.

3 HYNIX'S MAIN ARGUMENT IN ITS PAPERS IS
4 THAT A PACKET, I DON'T THINK THIS IS NECESSARILY
5 TRUE, BUT THEY SAY THAT A PACKET NEEDS TO BE
6 RECEIVED OVER MULTIPLE CLOCK CYCLES BECAUSE THAT'S
7 THE FORM THAT A PACKET TAKES IN RAMBUS'S PREFERRED
8 EMBODIMENT.

9 WELL, THOSE FOUR BITS ARE NOT RECEIVED ON
10 THE MULTIPLE CLOCK CYCLES. THEY ARE RECEIVED, IN
11 THIS CASE, OVER ONE BUS CYCLE, WHICH IN THE RAMBUS
12 PREFERRED EMBODIMENT IS HALF A CLOCK CYCLE.
13 THEY'RE ALL RECEIVED IN PARALLEL.

14 AND THE FEDERAL CIRCUIT, ON THIS POINT,
15 SIDED WITH RAMBUS. THEY SAID THAT THAT'S RIGHT,
16 THAT A READ REQUEST DOESN'T NEED TO BE THE WHOLE
17 PACKET. IN THE PREFERRED EMBODIMENT, THE READ
18 REQUEST DOES CORRESPOND TO THESE FOUR BITS OF THE
19 ACCESS TYPE.

20 AND THEN BASED ON THAT, THEY CAME UP WITH
21 THEIR CONSTRUCTION.

22 NUMBER 66, AGAIN, IF WE COULD GO BACK TO
23 THAT.

24 NOW, OBVIOUSLY IF THE FEDERAL CIRCUIT HAD
25 MEANT TO RESTRICT THIS TO A PACKET, THEY COULD HAVE

1 SAID, "THE TERM 'READ REQUEST' CONTAINS A SERIES OF
2 BITS CONTAINED IN A PACKET."

3 THEY DID NOT SAY SO. THEY JUST SAID A
4 SERIES OF BITS. THEY USED QUITE GENERAL LANGUAGE.

5 WHAT THEY WERE LOOKING AT WHEN THEY SAID
6 THAT WAS THIS PARTICULAR FOUR BITS IN THIS REQUEST
7 PACKET, WHICH WAS THE EXAMPLE IN THE PREFERRED
8 EMBODIMENT.

9 BUT THEY, IN NO WAY IN THE LANGUAGE THEY
10 CHOSE, RESTRICTED IT TO THAT.

11 SO FIRST THEY DID NOT RESTRICT IT TO A
12 PACKET IN THE LANGUAGE THEY CHOSE.

13 SECOND, THE EXAMPLE THAT THEY WERE
14 CONSIDERING SHOWS THAT HYNIX'S ARGUMENT CANNOT BE
15 CORRECT THAT WHEN THEY SAID A SERIES OF BITS, THEY
16 MEANT RECEIVED OVER MULTIPLE CLOCK CYCLES, BECAUSE
17 THE EXAMPLE THAT THEY DISCUSSED AND THAT WAS ONE OF
18 THE FACTORS THAT EVENTUALLY LED THEM TO THEIR
19 CONSTRUCTION DIDN'T HAVE THE PARTICULAR SERIES OF
20 BITS RECEIVED OVER MULTIPLE CLOCK CYCLES.

21 I THINK THE OTHER, THE OTHER MAIN
22 ARGUMENT THAT HYNIX MAKES WITH RESPECT TO WHY ITS
23 ACCUSED DEVICES DO NOT INFRINGE, OTHER THAN THE
24 SERIES OF BITS POINT, IS THAT IN THEIR DEVICES,
25 THEIR READ COMMANDS, OR READ REQUESTS, DO NOT

1 IDENTIFY WHAT TYPE OF READ TO PERFORM.

2 AND AS WE POINTED OUT IN OUR PAPERS,
3 HYNIX'S DATA SHEETS VERY CLEARLY IDENTIFY TWO TYPES
4 OF READ COMMANDS: READ AND READ WITH AUTO
5 PRECHARGE.

6 AND IN MR. BROWN'S TUTORIAL, ONE OF HIS
7 GRAPHICS, IN FACT, VERY CLEARLY SHOWED THOSE TWO
8 TYPES.

9 IF WE COULD PULL UP PAGE 24 OF THE
10 TUTORIAL.

11 AND YOU'LL SEE HERE, YOUR HONOR, THAT
12 THERE ARE TWO READ COMMANDS SHOWN THAT MR. BROWN
13 IDENTIFIED, BOTH DESIGNATED AS RD.

14 BUT ON THE FIRST READ COMMAND, IF WE
15 FOLLOW THAT DOWN, ON THE FIRST READ COMMAND, THE
16 A10 LINE HERE IS LOW, AND ON THE SECOND READ
17 COMMAND, THE A10 LINE IS HIGH.

18 AND ON THIS ONE, IN FACT, IT'S HARD TO
19 READ HERE, BUT THIS ONE IS IDENTIFIED, THE SECOND
20 ONE, AS A READ WITH AUTO PRECHARGE.

21 THE FIRST ONE IS JUST A READ WITHOUT AUTO
22 PRECHARGE.

23 SO THERE ARE SHOWN ON THIS PARTICULAR
24 TIMING DIAGRAM TWO TYPES OF READS IDENTIFIED.

25 YOU KNOW, MR. BROWN, OVER ON THE

1 LEFT-HAND SIDE, HAS BRACKETED JUST THE FIRST FOUR
2 CONTROL SIGNALS.

3 BUT THE A10 BIT IS ALSO PART OF BOTH OF
4 THOSE READ OPERATIONS IDENTIFYING WHETHER IT'S A
5 READ WITHOUT AUTO PRECHARGE OR A READ WITH AUTO
6 PRECHARGE.

7 HYNIX HAS ARGUED THAT THOSE ARE NOT
8 REALLY TWO DIFFERENT TYPES OF READS BECAUSE
9 ESSENTIALLY YOU'LL GET THE SAME DATA BACK WHETHER
10 IT'S A READ WITHOUT AUTO PRECHARGE OR A READ WITH
11 AUTO PRECHARGE.

12 I THINK THERE ARE A COUPLE OF RESPONSES
13 TO THAT. ONE GOES BACK, AGAIN, TO WHAT THE FEDERAL
14 CIRCUIT WAS CONSIDERING WHEN IT CAME UP WITH ITS
15 CONSTRUCTION WHICH SAID THAT THE READ REQUEST
16 IDENTIFIES THE TYPE OF READ TO PERFORM.

17 AND IF WE COULD GO AGAIN TO NUMBER 65.

18 THE FEDERAL CIRCUIT DID LOOK AT THE
19 PREFERRED EMBODIMENT, CONSTRUED THE TERM IN LIGHT
20 OF THE PREFERRED EMBODIMENT, AND SAID THAT IN
21 THE -- AT THE BOTTOM OF THIS LITTLE QUOTE FROM THE
22 FEDERAL CIRCUIT DECISION, LOOKING AT THE ACCESS
23 TYPE, THAT FOUR-BIT FIELD THAT, IN THE PREFERRED
24 EMBODIMENT, IS THE READ REQUEST, THE FEDERAL
25 CIRCUIT SAID, THE LAST LINE HERE, "THE FIRST BIT

1 INSTRUCTS THE MEMORY DEVICE TO PERFORM A READ; THE
2 NEXT THREE BITS TELL THE DEVICE WHAT TYPE OF READ
3 TO PERFORM (E.G. PAGE READ, NORMAL ACCESS READ, ET
4 CETERA)."

5 AND I THINK IT'S INSTRUCTIVE TO LOOK AT
6 WHAT THAT E.G. AND THAT ET CETERA MEANT WHEN THE
7 FEDERAL CIRCUIT WAS DISCUSSING THE TYPE OF READ
8 SPECIFIED BY THE ACCESS TYPE.

9 IF WE COULD GO TO THE '263 PATENT AND GO
10 TO PAGE 21, AND UP TOWARDS THE TOP OF COLUMN 10.
11 THERE YOU GO, JUST BLOW THAT UP. GO A LITTLE BIT
12 FURTHER DOWN. STOP THERE.

13 AFTER TALKING ABOUT THE ACCESS TYPE IN
14 THE PREVIOUS PARAGRAPH, THE FEDERAL CIRCUIT --
15 SORRY, EXCUSE ME.

16 THE PATENT SPECIFICATION NOTES, "THE
17 METHOD OF THIS INVENTION PROVIDES FOR ACCESS MODE
18 CONTROLS SPECIFICALLY FOR THE DRAMS. ONE SUCH
19 ACCESS MODE DETERMINES WHETHER THE ACCESS IS PAGE
20 MODE OR NORMAL RAS ACCESS."

21 AND THAT'S THE PARTICULAR EXAMPLE OF A
22 TYPE THAT THE FEDERAL CIRCUIT MENTIONED IN ITS
23 OPINION, BUT IT SAID THAT THAT WAS AN EXAMPLE AND
24 THEN IT PUT IN THE ET CETERA.

25 AND IF WE COULD GO DOWN TO THE NEXT

1 PARAGRAPH, THE VERY BEGINNING OF THE NEXT PARAGRAPH
2 IN COLUMN 10. NO, NO, THE NEXT ONE. THERE.

3 "THE ACCESS MODE ALSO DETERMINES WHETHER
4 THE DRAM SHOULD PRECHARGE THE SENSE AMPLIFIERS OR
5 SHOULD SAVE THE CONTENTS OF THE SENSE AMPS."

6 THAT WAS ANOTHER TYPE OF READ
7 SPECIFICALLY DESIGNATED BY A BIT IN THAT ACCESS
8 TYPE FIELD THAT, IN THE PREFERRED EMBODIMENT,
9 CORRESPONDS TO READ REQUEST.

10 AND IF WE COULD GO TO THE NEXT PAGE, PAGE
11 22, IT'S MADE PERHAPS EVEN CLEARER THERE.

12 ON COLUMN 11 WHERE YOU SEE THAT TABLE, IF
13 YOU BLOW UP THE TABLE AND GO A FEW LINES UNDERNEATH
14 IT. KEEP GOING, KEEP GOING. STOP.

15 IF WE LOOK UNDER THE TABLE A FEW LINES
16 DOWN, IT SAYS ACCESS TYPE BIT NUMBER TWO, THAT'S
17 THE PAGE MODE/NORMAL SWITCH, AND ACCESS TYPE BIT
18 MODE NUMBER 3, THAT'S THE PRECHARGE/SAVE-DATA
19 SWITCH.

20 AND THAT PRECHARGE SAVE-DATA SWITCH IS
21 EXACTLY WHAT CORRESPONDS TO WITH OR WITHOUT AUTO
22 PRECHARGE ACCORDING TO HOW THAT BIT IS SET, SIMILAR
23 TO HOW THE A10 BIT IS SET IN HYNIX'S DEVICES, THE
24 PRECHARGE WILL OR WILL NOT TAKE PLACE AS PART OF
25 THE READ OPERATION.

1 HYNIX ALSO OVERSTATES THE CASE WHEN IT
2 SAYS THAT THE READ OPERATION, THE DATA THAT'S READ
3 OUT WILL NOT BE AFFECTED BY WHETHER YOU DO IT WITH
4 OR WITHOUT A PRECHARGE.

5 AND WE LOOKED AT THIS JUST BEFORE, IT'S
6 ACTUALLY ON ANOTHER POINT, BUT IF WE COULD PULL UP
7 THE SDRAM DEVICE OPERATION, AND GO TO PAGE 7 AND
8 BLOW UP THE TOP PART, THE TEXT UNDER AUTO
9 PRECHARGE, AND BLOW UP THE TIMING DIAGRAM, TOO,
10 PLEASE.

11 WELL, WE NOTICE A COUPLE OF THINGS. ONE
12 IS THAT THE AUTO PRECHARGE START OCCURS WHILE THE
13 READ DATA IS STILL COMING OUT. IT STARTS TO
14 PRECHARGE DURING THE READ OPERATION.

15 AND SECOND, WHAT I POINTED OUT BEFORE, A
16 READ OR WRITE COMMAND WITH AUTO PRECHARGE CANNOT BE
17 TERMINATED IN THE WAY THAT READ COMMANDS WITHOUT
18 AUTO PRECHARGE CAN BE.

19 SO, IN SHORT, THIS IS EXACTLY THE TYPE OF
20 READ THE FEDERAL CIRCUIT WAS LOOKING AT WHEN IT --
21 THIS IS ONE OF THE TYPES OF READS THE FEDERAL
22 CIRCUIT WAS LOOKING AT WHEN IT CAME UP WITH ITS
23 CONSTRUCTION.

24 THAT'S NOT IN ANY WAY TO SUGGEST THAT THE
25 FEDERAL CIRCUIT'S CONSTRUCTION IS RESTRICTED TO THE

1 PREFERRED EMBODIMENT, BUT IT SHOULD AT LEAST
2 INCLUDE IT GIVEN THAT THEY WERE LOOKING AT IT.

3 AND SECOND, HYNIX'S OWN DOCUMENTS CLEARLY
4 SHOW THAT THESE ARE TWO DIFFERENT TYPES OF READS.

5 THE COURT: OKAY.

6 MR. BROWN: THERE'S A LOT TO ADDRESS
7 HERE, YOUR HONOR, AND I WILL TRY AND DO IT IN A
8 RELATIVELY ORGANIZED FASHION.

9 THE COURT: OKAY.

10 MR. BROWN: THIS IS THE AGREED
11 DEFINITION, THE DEFINITION WHICH WAS ANNOUNCED BY
12 THE FEDERAL CIRCUIT.

13 THE FEDERAL CIRCUIT DID NOTE IN ITS
14 OPINION THAT RAMBUS SAID THAT THE READ REQUEST WAS
15 THE SAME AS THE OPERATION CODE.

16 THE FEDERAL CIRCUIT DID NOT ADOPT
17 RAMBUS'S DECISION.

18 INSTEAD, THEY CAME UP WITH THIS DECISION,
19 WITH THIS CONSTRUCTION OF THE TERM "READ REQUEST."

20 NOW, I DO NOT THINK THAT THIS REQUIRES
21 NECESSARILY THAT IT, THAT THE READ REQUEST BE IN A
22 PACKET.

23 BUT I'M GOING -- I TAKE THE FEDERAL
24 CIRCUIT AT FACE VALUE THAT IT DOES REQUIRE THAT A
25 READ REQUEST BE A SERIES OF BITS. IT MIGHT NOT BE

1 IN A PACKET. IT MIGHT BE, YOU KNOW, ONE BIT OR,
2 YOU KNOW, A COUPLE OF BITS IN ONE CLOCK CYCLE AND
3 THEN SOME NUMBER OF CLOCK CYCLES LATER, IT MIGHT BE
4 ANOTHER NUMBER OF BITS, SOMETHING LIKE THAT.

5 BUT IT HAS TO BE A TIMED SERIES OF BITS,
6 AND THERE'S NO BASIS, IN MY VIEW, FOR SAYING THAT A
7 SERIES CAN BE A READ COMMAND, EVEN WITH THE A10
8 BIT.

9 THE READ COMMAND IS THE COMMAND ON RAS,
10 CAS, WRITE ENABLED CHIP SELECT, AND EVEN INCLUDING
11 THE A10 BIT, THEY ALL ARE READ IN SIMULTANEOUSLY.

12 THAT'S THE ONLY THING THAT RAMBUS HAS
13 ACCUSED OF BEING A READ REQUEST, AND I ASSUME THAT
14 THERE IS GOOD REASON WHY THEY HAVE DONE THAT.

15 BUT THERE IS NO WAY THAT THOSE, EVEN IF
16 YOU SAY ALL FIVE BITS ARE A PART OF THE READ
17 REQUEST, THAT THOSE ARE IN SERIES, OKAY.

18 AND I DON'T THINK -- I DON'T THINK THAT
19 THE FEDERAL CIRCUIT NECESSARILY MEANT THAT IT HAD
20 TO BE IN A PACKET.

21 BUT I THINK IT IS VERY CLEAR THAT THE
22 FEDERAL CIRCUIT HAD IN MIND THAT IT WAS A SERIES OF
23 BITS, AND THEY NOTED RAMBUS'S CONTENTION AS TO WHAT
24 A READ REQUEST MEANT AND THEY REJECTED IT AND
25 INSTEAD THEY CAME UP -- AND THEY CAME UP WITH THIS

1 CONSTRUCTION.

2 NOW, I'M NOT GOING TO DO A LOT OF
3 SPECULATION HERE AS TO HOW THE FEDERAL CIRCUIT
4 ARRIVED AT THIS PARTICULAR CONSTRUCTION BECAUSE I'M
5 NOT SURE THAT THERE'S A LOT OF EXPLANATION OF HOW
6 THEY CAME UP WITH THIS, AND MANY OF RAMBUS'S
7 EXPLANATIONS OF HOW THE FEDERAL CIRCUIT REACHED
8 THIS DECISION ARE JUST PURE SPECULATION.

9 HOWEVER, I WILL TAKE THE FEDERAL CIRCUIT
10 AT FACE VALUE ON THIS WITH A CONSTRUCTION WHICH IS
11 BINDING ON RAMBUS THAT IT DOES REQUIRE A SERIES --
12 THAT A READ REQUEST DOES REQUIRE A SERIES OF BITS,
13 AND I DON'T THINK THAT THERE IS ANY SUPPORTABLE
14 POSITION THAT A SERIES OF BITS COULD BE ANYTHING
15 MORE OR ANYTHING LESS THAN BITS THAT COME IN AT
16 DIFFERENT TIMES.

17 THEY MAY NOT HAVE TO BE, YOU KNOW, ONCE A
18 CLOCK CYCLE. THEY MAY NOT HAVE TO BE ONE BIT PER
19 CLOCK CYCLE OR ONE BIT AT A TIME, BUT THERE DOES
20 HAVE TO BE A TIME SEQUENCE OF BITS INPUT.

21 SECOND. YES, THE FEDERAL CIRCUIT SAYS
22 THE REQUEST HAS TO IDENTIFY WHAT TYPE OF READ TO
23 PERFORM, NOT WHAT KIND OF ACCESS, NOT WHAT KIND OF
24 MODE TO, TO PUT THE MEMORY INTO, BUT WHAT TYPE OF
25 READ TO PERFORM.

1 AND THE -- IT'S VERY CLEAR FROM THE
2 FEDERAL CIRCUIT OPINION THAT THE ONLY TWO TYPES OF
3 READS THAT WERE ACTUALLY IDENTIFIED IN THAT OPINION
4 ARE A NORMAL MODE READ AND A PAGE MODE READ, AND
5 THOSE ARE TWO DIFFERENT TYPES OF READS BECAUSE, IF
6 YOU REMEMBER LAST THURSDAY, WE -- IN THE TUTORIAL
7 WE TALKED BRIEFLY ABOUT WHAT THE DIFFERENCE IS
8 BETWEEN A NORMAL MODE READ AND A PAGE MODE READ, AT
9 LEAST WITHIN THE CONTEXT OF THE PREFERRED
10 EMBODIMENT OF THE PATENTS.

11 AND IN A NORMAL -- A REQUEST PACKET HAS
12 THE SAME FORMAT IN BOTH OF THOSE CASES.

13 BUT IN THE NORMAL MODE READ, THE DEVICE,
14 THE MEMORY DEVICE HAS TO KNOW TO FIRST EXTRACT THE
15 ROW ADDRESS, ACTIVATE THE ROW, THEN USING A COLUMN
16 ADDRESS EXTRACTED FROM THE PACKET, CHOOSE THE BITS
17 FROM THE PARTICULAR COLUMNS. THAT'S A NORMAL MODE
18 READ.

19 NOW, IN A PAGE MODE READ, THE PACKET HAS
20 THE SAME REQUEST FORMAT, BUT BASICALLY BECAUSE
21 THERE IS A ROW ALREADY OPEN, THE PACKET -- OR THE
22 MEMORY CHIP NEEDS TO KNOW JUST TO EXTRACT THE
23 COLUMN ADDRESS, USE THAT COLUMN ADDRESS TO SELECT
24 THE BITS TO COME FOR OUTPUT.

25 BUT BECAUSE, AGAIN, IN THE PREFERRED

1 EMBODIMENT, BECAUSE THE PACKET HAS THE SAME FORMAT
2 FOR WHETHER IT'S A PAGE MODE READ OR A NORMAL MODE
3 READ, THAT IS, IT HAS THE SAME, BASICALLY THE SAME
4 NUMBER OF BITS IN THE ADDRESS IN THE PACKET, THE
5 PACKET HAS TO TELL THE MEMORY CHIP WHETHER THIS IS
6 A NORMAL MODE READ OR WHETHER THIS IS A PAGE MODE
7 READ, AND THOSE ARE THE ONLY TYPES OF READS THAT
8 WERE MENTIONED IN THE FEDERAL CIRCUIT OPINION.

9 NOW, YES, THE FEDERAL CIRCUIT USED AN
10 E.G. AND THEY USED AN ET CETERA.

11 OKAY. BUT THEY DIDN'T TELL US -- UNLIKE
12 RAMBUS'S SPECULATION, THEY DIDN'T TELL US WHAT THAT
13 ET CETERA MEANT.

14 AND IF YOU GO BACK TO WHAT MR. DETRE TOLD
15 YOU FROM THE, OR POINTED OUT FROM THE, FROM THE
16 '263 PATENT, BASICALLY HE WAS TALKING ABOUT ACCESS
17 MODE CONTROL, AND THOSE THREE BITS THAT HE'S USING,
18 YES, ARE USED IN ACCESS MODE CONTROL.

19 BUT AN ACCESS MODE IS NOT THE SAME AS A
20 TYPE OF READ. THERE'S NO -- I MEAN, THIS IS
21 BASICALLY -- THE ACCESS MODE CONTROL IS CONTROLLING
22 THE OPERATIONS THAT ARE GOING TO OCCUR DURING
23 WHATEVER ACCESS IS BEING REQUESTED.

24 IN ONE OF THOSE, ONE OF THOSE THINGS IN
25 THE RAMBUS PATENT, AND ACTUALLY THERE'S AN ANALOGY

1 IN THE SDRAM WHICH I'M GOING TO COME TO IN JUST A
2 MINUTE, BUT BASICALLY THERE ARE TWO TYPES OF READS
3 THAT ARE SPECIFIED. THERE'S A NORMAL MODE AND
4 THERE'S A PAGE MODE. THERE'S AT LEAST THOSE.

5 NOW, THE ACCESS MODE, ONE OF THESE BITS,
6 ALSO SAYS AFTER YOU'RE DONE WITH THIS READ,
7 PRECHARGE OR SAVE THE DATA.

8 OKAY. IT BASICALLY -- PART OF THIS
9 ACCESS MODE CONTROL IS TO TELL THE CHIP WHAT TO DO
10 AFTER THE READ OPERATION IS COMPLETE.

11 AND THAT'S WHAT HAPPENS IN SDRAMS ALSO,
12 OKAY, THIS A10 BIT. IT BASICALLY SAYS WHAT TO DO
13 AFTER THE READ OPERATION IS COMPLETE.

14 AND THE SLIDE FROM MY TUTORIAL THAT
15 MR. DETRE SHOWED YOU -- AND I MAY EVEN ACTUALLY BE
16 ABLE TO FIND IT -- I THINK THIS IS THE ONE THAT
17 MR. DETRE SHOWED YOU, OKAY, THAT, YES, THERE'S A
18 READ BANK -- THERE'S ONE READ COMMAND THAT'S JUST A
19 READ WITH THE A10 BIT INACTIVE, AND THEN THERE'S
20 ANOTHER READ COMMAND WITH THE A10 BIT ACTIVE, OKAY,
21 WHICH MR. DETRE IS BASICALLY INDICATING IS A READ
22 WITH AUTO PRECHARGE, OKAY.

23 IT CERTAINLY LOOKS TO ME AS IF THE DATA
24 THAT COMES OUT IN RESPONSE TO THOSE TWO READ
25 COMMANDS IS PRETTY MUCH THE SAME.

1 THE DIFFERENCE OF THE A10 BIT IS THAT
2 AFTER THE READ OF DATA IS COMPLETED, IT SPECIFIES
3 ANOTHER OPERATION THAT SHOULD OCCUR AFTER THAT
4 POINT. IT DOESN'T CHANGE THE TYPE OF READ.

5 AND I CAN ILLUSTRATE THAT. THERE ARE TWO
6 WAYS OF DOING THIS, OKAY, AND THIS IS -- THE TOP
7 DIAGRAM IS THE ONE THAT MR. DETRE TOLD YOU, OR
8 SHOWED YOU, FOR ONE OF THE TIMING DIAGRAMS, AND IT
9 IS THAT YOU COULD SEND A BURST READ WITH AUTO
10 PRECHARGE, AND THIS BASICALLY IS A READ COMMAND,
11 SIMULTANEOUSLY WITH THE FOUR BITS IN THE READ
12 COMMAND, AND THE A10 BIT IS SECOND. OKAY. SO THAT
13 BECOMES A READ WITH AUTO PRECHARGE OPERATION.

14 NOW, YOU CAN DO EXACTLY THE SAME THING
15 WITH TWO SEPARATE COMMANDS. YOU CAN SEND IN THE
16 READ COMMAND WITH THE A10 BIT NOT SET, AND THEN
17 JUST BEFORE THE END OF THE BURST, YOU SEND A
18 PRECHARGE COMMAND AND EXACTLY THE SAME THING
19 HAPPENS.

20 BUT INSTEAD WHAT YOU'VE DONE IS YOU'VE
21 COMMANDED ONE OPERATION WITH THE READ COMMAND AND
22 YOU'VE COMMANDED ANOTHER OPERATION WITH THE
23 PRECHARGE COMMAND.

24 WHEN YOU SEND IN A READ WITH THE A10, OR
25 A READ COMMAND WITH THE A10 BIT SET, YOU'RE

1 BASICALLY TELLING THE DEVICE TO DO TWO OPERATIONS,
2 FIRST DO THE READ, THEN DO THE PRECHARGE.

3 OKAY. SO THE A10 BIT, IN OUR VIEW, IN
4 HYNIX'S VIEW, DOES NOT -- IT IS NOT SOMETHING THAT
5 SPECIFIES A TYPE OF READ TO PERFORM, AND THAT'S NOT
6 INCONSISTENT WITH EITHER THE PATENT SPECIFICATION
7 OR WITH THE FEDERAL CIRCUIT'S, THE FEDERAL
8 CIRCUIT'S DISCUSSION.

9 NOW, I DO WANT TO GO BACK AND ANSWER A
10 QUESTION THAT I DIDN'T HEAR MR. DETRE ANSWER.
11 THERE IS NO DISCLOSURE IN THE PATENT OF AN OP CODE
12 BEING TRANSMITTED TO THE DEVICE IN ANY WAY OTHER
13 THAN WITHIN A PACKET. THERE'S NO SUGGESTION THAT
14 AN OP CODE CAN BE TRANSMITTED IN ANY WAY OTHER THAN
15 THE PACKET.

16 AND MR. DETRE IS CORRECT THAT YOU DON'T
17 HAVE TO DISCLOSE EVERYTHING THAT IS KNOWN.

18 BUT THE RELEVANT INQUIRY UNDER SECTION
19 112 IS WHETHER OR NOT THE INVENTION, AS CLAIMED,
20 OKAY, THAT IS IN THE GRANTED CLAIM AND WHICH IS THE
21 GRANTED CLAIM AS CONSTRUED BY THE COURT, WHETHER
22 THAT IS DISCLOSED IN THE SPECIFICATION, EITHER
23 EXPRESSLY OR INHERENTLY.

24 AND IF YOU DIVORCE -- THERE IS NO
25 DISCLOSURE OF AN OPERATION CODE OUTSIDE OF THE USE

1 OF A PACKET.

2 AND MR. MURPHY AGREED WITH THAT IN HIS --
3 IT'S HERE SOMEWHERE. MR. MURPHY AGREED WITH THAT
4 IN HIS DEPOSITION.

5 "IS THERE ANY DISCLOSURE IN THE PATENT OF
6 AN OPERATION CODE THAT IS NOT CONTAINED IN A
7 PACKET?"

8 AND HE AGREED THAT IN THE PREFERRED
9 EMBODIMENT, ALL OF THE OP CODES ARE DELIVERED OVER
10 THE -- OR DELIVERED IN A PACKET.

11 NOW, HE ALSO SAYS THAT HE BELIEVES ONE OF
12 ORDINARY SKILL IN THE ART WOULD UNDERSTAND THAT IT
13 DOESN'T HAVE TO BE DELIVERED IN A PACKET.

14 BUT ON THE OTHER HAND, THERE'S NO OTHER
15 WAY, THERE'S NO DISCLOSURE IN THE PATENT, AND
16 MR. MURPHY AGREED THAT THERE'S NO DISCLOSURE OF AN
17 OP CODE BEING DELIVERED IN SOME WAY OTHER THAN IN A
18 PACKET.

19 NOW, SO IN ORDER TO MEET THE WRITTEN
20 DESCRIPTION REQUIREMENT, THERE HAS TO BE SOME
21 DISCLOSURE. IT'S EITHER EXPRESS OR BY PRINCIPLES
22 OF INHERENCE, NOT -- OR BY PRINCIPLES OF INHERENCY
23 THAT THE INVENTION AS CLAIMED, AS NOW CLAIMED, THAT
24 IS THE OPERATION DIVORCED FROM A PACKET, OKAY, IS
25 BASICALLY WHAT THEY'RE SAYING A CLAIM IS NOW, OKAY,

1 WAS IN POSSESSION OF THE INVENTORS AT THE TIME OF
2 THE ORIGINAL FILING.

3 AND THERE IS NO SUCH DISCLOSURE.

4 THE MOST THAT RAMBUS CAN SAY IS, FROM OUR
5 DISCLOSURE OF AN OPERATION CODE IN A PACKET, IT'S
6 OBVIOUS TO ONE OF ORDINARY SKILL IN THE ART THAT
7 THE OPERATION CODE CAN BE DELIVERED IN OTHER WAYS.

8 BUT THAT'S NOT THE TEST. THE FEDERAL
9 CIRCUIT HAS SAID IN LOCKWOOD VERSUS AMERICAN
10 AIRLINES, HAS SAID IN DELAVAL V. GENERAL ELECTRIC,
11 THAT WHETHER SOMETHING IS OBVIOUS IN VIEW OF THE
12 DISCLOSURE IS NOT THE CORRECT TEST UNDER THE
13 WRITTEN DESCRIPTION REQUIREMENT.

14 THERE HAS TO BE A DISCLOSURE WHICH IS
15 EXPRESS OR WHICH IS INHERENT.

16 AND YES, IT'S A DISCLOSURE AS VIEWED BY
17 ONE OF ORDINARY SKILL IN THE ART, BUT THE, THE
18 DISCLOSURE HAS TO BE IN THE SPECIFICATION.

19 THE COURT: SO UNDER THE WRITTEN
20 DESCRIPTION REQUIREMENT, IF SOMEONE READING A
21 PATENT, IF EVERYBODY WOULD KNOW, "OH, THIS SAYS IT
22 NEEDS TO BE IN, OR IT IS IN A PACKET, BUT WE ALL
23 KNOW YOU CAN DO IT OTHERWISE," THAT WRITTEN
24 DESCRIPTION IS INSUFFICIENT TO SUPPORT IT?

25 MR. BROWN: THERE HAS TO BE SOMETHING IN

1 THE WRITTEN DESCRIPTION, IN THE WRITTEN DESCRIPTION
2 THAT SAYS, YOU KNOW, "WE'VE SHOWN THIS OPERATION
3 CODE IN A PREFERRED EMBODIMENT. THOSE OF ORDINARY
4 SKILL IN THE ART WILL UNDERSTAND THAT AN OPERATION
5 CODE CAN BE TRANSMITTED IN OTHER WAYS," FOR
6 EXAMPLE.

7 OKAY. THAT KIND OF A DISCLOSURE IS NOT
8 IN THIS SPECIFICATION.

9 I THINK THAT ANSWERS THE QUESTION.

10 THE COURT: YEAH.

11 MR. BROWN: MR. DETRE, AND RAMBUS, OVER
12 QUITE A BIT OF TIME NOW, HAS SPENT -- HAS
13 REPEATEDLY SAID THAT THERE ARE MULTIPLE INVENTIONS
14 DISCLOSED IN THESE PATENTS, AND I'LL AGREE THAT
15 THERE ARE MULTIPLE INVENTIONS DISCLOSED IN THESE
16 PATENTS, OKAY.

17 BUT EVEN AGREEING TO THAT, AGREEING THAT
18 THERE ARE MULTIPLE INVENTIONS DISCLOSED IN THESE
19 PATENTS SAYS NOTHING ABOUT WHAT THOSE INVENTIONS
20 ARE.

21 WHAT'S IMPORTANT IS WHAT IS IN THE
22 CLAIMS.

23 BUT I DO WANT TO GO BACK AND TAKE ISSUE
24 WITH A COUPLE OF THINGS THAT MR. DETRE HAS SAID,
25 AND THAT IS THAT BACK IN THE ORIGINAL CLAIMS, THERE

1 WAS SOMETHING LIKE -- IN THE CLAIMS AS ORIGINALLY
2 FILED, THERE WERE, I THINK, 25 DIFFERENT
3 INDEPENDENT CLAIMS AND THERE WAS A RESTRICTION
4 REQUIREMENT THAT WAS ISSUED.

5 THERE -- AND THERE WAS A RESTRICTION
6 REQUIREMENT BASICALLY, WHICH IS THE PATENT OFFICE
7 PROCEDURE BY WHICH BASICALLY THE EXAMINER SAYS "I
8 ONLY WANT TO EXAMINE THIS SET OF CLAIMS IN THIS SET
9 OF APPLICATIONS. IF YOU WANT ME TO EXAMINE THE
10 NEXT SET OF CLAIMS, YOU HAVE TO FILE ANOTHER
11 APPLICATION."

12 AND THERE WAS AN 11 WAY RESTRICTION
13 REQUIREMENT. SORRY, THAT'S A PATENTESE THING.

14 OF THOSE 11 SETS OF CLAIMS THAT THE
15 EXAMINER REQUIRED THEM TO DIVIDE OUT, NINE OF THOSE
16 SETS OF CLAIMS, THAT IS, ALL BUT TWO OF THE
17 INDEPENDENT CLAIMS THAT WERE IN THAT APPLICATION
18 REQUIRED, RECITED SPECIFICALLY A BUS WHICH
19 COMPRISED A SET OF SIGNAL LINES OVER WHICH
20 SUBSTANTIALLY ALL ADDRESS DATA AND CONTROL NEEDED
21 FOR COMMUNICATION WITH THE OTHER DEVICES IS
22 TRANSMITTED, AND IN WHICH THE NUMBER OF BITS IN A
23 SINGLE ADDRESS IS -- SORRY -- THE NUMBER OF BUS
24 LINES IS SUBSTANTIALLY FEWER THAN THE NUMBER OF
25 BITS IN A SINGLE ADDRESS.

1 THEY WERE -- I MEAN, ALL BUT TWO OF THE
2 INDEPENDENT CLAIMS HAD BOTH OF THOSE LIMITATIONS IN
3 THEM.

4 BUT NEVERTHELESS, THERE -- THOSE, THOSE
5 REMAINING 23 CLAIMS WERE DIVIDED UP INTO NINE
6 DIFFERENT INVENTIONS.

7 WHY WERE THEY DIVIDED UP INTO NINE
8 DIFFERENT INVENTIONS?

9 IT'S BECAUSE THERE ARE OTHER FEATURES,
10 SUCH AS AN ACCESS TIME REGISTER, SUCH AS A PACKET
11 PROTOCOL, SUCH AS THE VARIABLE BLOCK SIZE
12 INFORMATION, THAT CAN BE USED WITH THAT KIND OF A
13 BUS, BUT DON'T NECESSARILY HAVE TO BE USED WITH
14 THAT KIND OF A BUS.

15 SO THE DIFFERENT INVENTIONS WERE, BY AND
16 LARGE, THIS PARTICULAR DEFINED BUS, OR THE BUS
17 DEFINED BY THOSE TWO REQUIREMENTS, IN COMBINATION
18 WITH SOME OF THESE SUBFEATURES, LIKE BLOCK SIZE,
19 LIKE AN ACCESS TIME REGISTER, LIKE A PACKET, THAT
20 COULD BE USED WITH THIS BUS, THAT COULD BE USED IN
21 COMBINATION, THAT IS, YOU COULD HAVE TWO OF THESE
22 SUBFEATURES WITH THAT ONE BUS.

23 BUT IN ALL CASES, THE DIFFERENT
24 INVENTIONS WERE THIS, WHAT WE'VE BEEN CALLING, WHAT
25 I'VE BEEN CALLING ANYWAY, A NARROW MULTIPLEXED BUS

1 IN COMBINATION WITH ONE OF THESE OTHER THINGS.

2 NOW, RAMBUS IS USING THIS NOW TO EXALT
3 THE COMBINATION OF AN ACCESS TIME REGISTER WITH THE
4 NARROW BUS, OR, SORRY, TO EXALT THE ACCESS TIME
5 REGISTER ITSELF, RATHER THAN A SUBFEATURE THAT CAN
6 BE USED WITH THE NARROW MULTIPLEXED BUS, THEY'RE
7 EXALTING IT TO AN INVENTION ON ITS OWN.

8 THEY'RE DOING THE SAME THING WITH BLOCK
9 SIZE INFORMATION, AND THEY'RE DOING THE SAME THING
10 WITH AN OPERATION CODE.

11 THERE IS AN OPERATION CODE THAT'S
12 MENTIONED IN ONE OR MORE OF THE CLAIMS OF THE
13 ORIGINAL APPLICATION, AND I CAN'T HONESTLY TELL YOU
14 WHICH ONE IT IS RIGHT NOW.

15 BUT BASICALLY IT TALKS ABOUT HAVING AN
16 OPERATION CODE IN A PACKET ON THIS KIND OF A BUS
17 THAT BASICALLY TRANSMITS A READ, OR TELLS THE
18 DEVICE, OR TELLS THE MEMORY TO DO A READ OPERATION.

19 PARTICULARLY IN THE CONTEXT OF THE
20 STATEMENTS IN THE SPECIFICATION THAT THE INVENTION
21 IS A BUS ARCHITECTURE AND A SUBSYSTEM THAT INCLUDES
22 THE FEATURE THAT ALL ADDRESS DATA IN CONTROL IS
23 TRANSMITTED, OR SUBSTANTIALLY ALL ADDRESS DATA IN
24 CONTROL IS SUBMITTED, IS TRANSMITTED OVER THE SET
25 OF BUS LINES, AND THE BUS WHICH, WHERE THE NUMBER

1 OF BITS IN AN ADDRESS IS SUBSTANTIALLY GREATER THAN
2 THE NUMBER OF LINES IN THE BUS, PARTICULARLY IN
3 VIEW OF THAT LANGUAGE, THAT THAT IS THE INVENTION,
4 OR THE CHARACTERIZATION OF THE INVENTION, ONE OF
5 ORDINARY SKILL WOULD NOT READ THAT SPECIFICATION
6 WHEN IT COMES DOWN TO THE PARTICULAR PACKET
7 PROTOCOL AND THE MENTION, ONE MENTION, TWO MENTIONS
8 ACTUALLY, OF AN OP CODE THAT ARE WITHIN THAT
9 PACKET, ONE OF ORDINARY SKILL IN THE ART WOULD NOT
10 TAKE THAT AS A DISCLOSURE THAT THE OP CODE CAN BE
11 TAKEN OUT OF THE PACKET, CAN BE TAKEN OUT OF THE
12 PACKET PROTOCOL, CAN BE TAKEN OUT OF THE BUS
13 ARCHITECTURE AND SORT OF SET ASIDE AS A COMPLETELY
14 SEPARATE INVENTION, WHICH IS WHAT RAMBUS IS TRYING
15 TO DO NOW.

16 AND THE FACT IS THAT THERE IS NO
17 DISCLOSURE IN THE SPECIFICATION AS FILED OF AN
18 OPERATION CODE, EXCEPT IN THE CONTEXT OF A PACKET.

19 THE COURT: AND YOU WOULD DEFINE "PACKET"
20 HOW?

21 MR. BROWN: IT'S, AGAIN, ONE OF THOSE
22 THINGS THAT I CAN CERTAINLY GIVE YOU EXAMPLES OF A
23 PACKET, AND YOU'VE PROBABLY LOOKED AT FIGURE 4 OF
24 THIS PATENT MORE OFTEN THAN YOU WOULD CARE TO, SO
25 I'M NOT GOING TO MAKE YOU LOOK AT IT AGAIN.

1 BUT A PACKET IS A SET OF RELATED
2 INFORMATION, OKAY, THAT IS AT LEAST LOGICALLY
3 RELATED; THAT IS, THAT IT'S A SET OF INFORMATION
4 THAT GOES TOGETHER, OKAY, THAT IS TRANSMITTED IN
5 SOME KIND OF A SEQUENCE OVER THE BUS.

6 THE COURT: OKAY.

7 MR. BROWN: OKAY?

8 THE COURT: YES.

9 ALL RIGHT. LET'S TAKE A BREAK.

10 MR. BROWN: OKAY.

11 THE COURT: WHY DON'T WE TRY AND BE BACK
12 AT TEN OF 4:00.

13 (WHEREUPON, A RECESS WAS TAKEN.)

14 THE COURT: I DON'T WANT TO GET SIDE
15 TRACKED, BUT LET ME JUST READ, AND THIS IS ACTUALLY
16 FROM THE NORTHERN DISTRICT MODEL INSTRUCTIONS, AN
17 INSTRUCTION ON WRITTEN DESCRIPTION.

18 IT READS, IN PART, "THE WRITTEN
19 DESCRIPTION REQUIREMENT IS SATISFIED IF PERSONS OF
20 ORDINARY SKILL IN THE FIELD WOULD RECOGNIZE FROM
21 THE PATENT APPLICATION AS FIRST FILED THAT THE
22 INVENTOR HAD IN MIND AT THAT TIME THE FULL SCOPE OF
23 THE INVENTION AS FINALLY CLAIMED IN THE PATENT.

24 A REQUIREMENT IN A CLAIM NEED NOT BE
25 SPECIFICALLY DISCLOSED IN THE ORIGINAL PATENT

1 APPLICATION IF PERSONS OF ORDINARY SKILL IN THE
2 FIELD, READING THAT APPLICATION, WOULD UNDERSTAND
3 THAT THE MISSING REQUIREMENT MUST NECESSARILY BE
4 PRESENT."

5 DO EITHER OF YOU QUARREL WITH THAT AS AN
6 ACCURATE STATEMENT OF THE LAW?

7 MR. DETRE: I DON'T, YOUR HONOR.

8 MR. BROWN: NO.

9 THE COURT: SO DOESN'T THIS QUESTION AS
10 TO COMMUNICATION OTHER THAN IN A PACKET WOULD BE
11 RECOGNIZED AS SOMETHING THAT MUST NECESSARILY BE
12 PRESENT IN THE INVENTION AS DISCLOSED?

13 MR. BROWN: THAT IS CORRECT, YOUR HONOR.

14 MR. DETRE: COULD I ADDRESS THAT, AND
15 MAYBE ALSO SOME OF THE OTHER POINTS MR. BROWN MADE?

16 THE COURT: BUT DO YOU AGREE THAT THAT'S
17 THE QUESTION?

18 MR. DETRE: I AGREE THAT THAT'S THE
19 QUESTION.

20 BUT WITH RESPECT TO DISTINCT INVENTIONS
21 IN THIS CASE, SO WE HAVE TO LOOK AT THE INVENTIONS
22 SEPARATELY AND UNDERSTAND, WITH RESPECT TO THE
23 DISTINCT INVENTIONS, WHETHER A PERSON OF ORDINARY
24 SKILL WOULD UNDERSTAND THAT, WITH RESPECT TO THAT
25 DISTINCT INVENTION, SOME FORM OF OPERATION CODE

1 MUST NECESSARILY BE SENT, AND IT NEED NOT BE
2 RESTRICTED TO THE KIND OF OPERATION CODE IN ONE OF
3 THE OTHER DISTINCT INVENTIONS.

4 THE COURT: OKAY. I THINK I UNDERSTAND
5 BOTH YOUR ARGUMENTS ON THAT, BUT LET ME ASK, BEFORE
6 I LET YOU GO FURTHER, WHAT OF THE REST OF THE
7 MOTIONS ARE YOU PARTICULARLY ANXIOUS TO ADDRESS?

8 MR. BROWN: I THINK WE'RE PARTICULARLY,
9 ON THE -- WE SHOULD TALK ABOUT THE FIRST AND SECOND
10 EXTERNAL CLOCK ISSUE.

11 THE COURT: OKAY. YEAH, THAT'S ONE I'M
12 INTERESTED IN.

13 WHAT ARE YOU PARTICULARLY INTERESTED IN
14 ADDRESSING?

15 MR. DETRE: IF YOUR HONOR DOESN'T HAVE
16 ANY PARTICULAR CONCERNS ABOUT OTHER ISSUES, I DON'T
17 THINK WE NEED TO ADDRESS ANY OF THEM AND WE'LL
18 STAND ON OUR PAPERS.

19 THE COURT: OKAY. DO YOU WANT TO --

20 MR. DETRE: I MIGHT SAY ACTUALLY, I'LL
21 TAKE THAT BACK, MAYBE ON SYNCHRONOUS MEMORY DEVICE
22 I HAVE A FEW THINGS TO SAY.

23 THE COURT: OKAY. WHY DON'T YOU GO AHEAD
24 AND MAKE THE ADDITIONAL COMMENTS YOU WANTED TO ON
25 THE ISSUE THAT YOU STARTED TO TALK ABOUT,

1 RECOGNIZING THAT I THINK I UNDERSTAND IT, AND THEN
2 WE'LL GO TO THE CLOCKS AND WE'LL END WITH THE
3 SYNCHRONOUS MEMORY DEVICE.

4 MR. DETRE: THANK YOU, YOUR HONOR.

5 I MAY HAVE SAID THIS BEFORE, BUT I JUST
6 WANTED TO POSSIBLY REITERATE ONE POINT IN RESPONSE
7 TO SOMETHING MR. BROWN SAID ABOUT ACCESS MODES AND
8 ACCESS TYPES, AND THAT IS THAT THE PATENT
9 SPECIFICATION IS QUITE CLEAR THAT THE ACCESS MODE
10 IS DETERMINED BY THE ACCESS TYPE FIELD, AND THAT
11 ACCESS TYPE FIELD IS FOUR BITS, WHICH IN THE
12 PREFERRED EMBODIMENT ARE ALL RECEIVED IN PARALLEL,
13 AND THAT'S WHAT THE FEDERAL CIRCUIT FOUND FOR AN
14 EMBODIMENT TO CORRESPOND TO A READ REQUEST.

15 THE SECOND POINT --

16 THE COURT: WHAT LANGUAGE DO YOU THINK
17 SUPPORTS THAT LAST STATEMENT?

18 MR. DETRE: OH, IN THE SPECIFICATION THAT
19 THE --

20 THE COURT: NO, THAT THE FEDERAL CIRCUIT
21 FOUND THAT TO BE A READ REQUEST?

22 MR. DETRE: OH. LET ME GO TO THE FEDERAL
23 CIRCUIT OPINION.

24 THE FEDERAL CIRCUIT, AT THE BEGINNING --
25 AT THE TOP OF PAGE 1092 IN THE OPINION, AFTER

1 COMPARING THE PARTIES' RESPECTIVE POSITIONS, THE
2 FEDERAL -- LET ME START THERE, ACTUALLY, ON PAGE
3 1091. THE FEDERAL CIRCUIT IS COMPARING THE
4 PARTIES' RESPECTIVE POSITIONS AND NOTES THAT
5 INFINEON ARGUED THAT THE READ REQUEST MUST CONTAIN
6 ALL INFORMATION NECESSARY TO PERFORM THE REQUESTED
7 READ, AND THEN NOTED THAT RAMBUS'S POSITION, TO THE
8 CONTRARY, WAS THAT THE READ REQUEST IN THE
9 PREFERRED EMBODIMENT IS, QUOTE, "ONE COMPONENT OF
10 THE REQUEST PACKET COMPRISING THE FIRST FOUR BITS
11 OF THE PACKET."

12 AND THEN THE FEDERAL CIRCUIT HAS THE
13 FIGURE 4 SHOWING --

14 PERHAPS WE CAN PULL THAT UP, FROM ANY OF
15 THE PATENTS, FIGURE 4. MOVE FORWARD A FEW PAGES.
16 THERE WE GO AT THE BOTTOM, FIGURE 4.

17 THE FEDERAL CIRCUIT REPRODUCED FIGURE 4
18 AND TALKED ABOUT, "AS SHOWN ABOVE, THE REQUEST
19 PACKET HAS MULTIPLE FIELDS, INCLUDING AN ACCESS
20 TYPE FIELD," AND THAT'S THE FIRST FOUR BITS ALL IN
21 THE TOP LINE OF THE PACKET, ONLY PART OF THE TOP
22 LINE OF THE PACKET.

23 AND THEN THE FEDERAL CIRCUIT PROCEEDS TO
24 ANALYZE WHETHER A READ REQUEST MUST CONTAIN MORE
25 INFORMATION THAN WHAT'S CONTAINED IN THE ACCESS

1 TYPE FIELD.

2 AND IT CONCLUDES NEAR THE TOP OF PAGE
3 1093. "CONTRARY TO INFINEON'S POSITION, IN ACCORD
4 WITH RAMBUS'S POSITION, THAT REFERENCES IN THE
5 SPECIFICATION TO READ REQUESTS DO NOT SUGGEST THE
6 PRESENCE OF ADDRESS AND CONTROL INFORMATION.

7 THE SPECIFICATION MERELY INDICATES THAT
8 THE READ REQUEST REQUESTS DATA FROM A MEMORY DEVICE
9 AND SPECIFIES WHAT TYPE OF READ (E.G., PAGE MODE,
10 NORMAL MODE, ET CETERA) TO PERFORM."

11 "MOREOVER," THE FEDERAL CIRCUIT GOES ON,
12 "THE DEPENDENT CLAIMS DEMONSTRATE THAT READ REQUEST
13 IS DISTINCT FROM A REQUEST PACKET."

14 SO THE FEDERAL CIRCUIT WAS CONSIDERING
15 INFINEON'S POSITION THAT THE READ REQUEST HAD TO BE
16 THE WHOLE REQUEST PACKET, RAMBUS'S POSITION THAT
17 THE READ REQUEST HAD TO BE JUST THAT ACCESS TYPE,
18 ZERO TO THREE, AND SIDED WITH RAMBUS THAT ALL OF
19 THIS OTHER INFORMATION, ADDRESS INFORMATION AND
20 CONTROL INFORMATION LIKE THE BLOCK SIZE -- AND
21 THAT'S ALL THERE IS ONCE YOU GET PAST THIS FIRST
22 LINE, ALL YOU'VE GOT IS ADDRESS INFORMATION AND
23 SOME CONTROL INFORMATION -- AND THE FEDERAL CIRCUIT
24 FOUND THAT THAT DID NOT NEED TO BE IN THE READ
25 REQUEST.

1 SO WHAT THE FEDERAL CIRCUIT WOUND UP
2 WITH, FOR PURPOSES OF THE PREFERRED EMBODIMENT, WAS
3 TO AGREE WITH RAMBUS THAT, IN THE PREFERRED
4 EMBODIMENT, ONLY THE ACCESS TYPE WHICH REQUESTS,
5 WHICH SPECIFIES THAT IT'S A READ AND IDENTIFIES THE
6 TYPE OF READ, IS THE READ REQUEST.

7 AND THAT'S WHAT IT WAS LOOKING AT WHEN IT
8 CAME UP WITH ITS CONSTRUCTION WHICH, WHICH SAID A
9 SERIES OF BITS.

10 SO THERE ARE THE SERIES. THEY'RE A
11 SERIES IN THE PREFERRED EMBODIMENT IN SPACE, A
12 SPACIAL SERIES, ONE NEXT TO THE OTHER, NOT IN TIME
13 ONE AFTER THE OTHER.

14 THE COURT: OKAY.

15 MR. DETRE: THE SECOND POINT I WANTED TO
16 MAKE, YOUR HONOR, AND I THINK, YOU KNOW, AS THE
17 MODEL INSTRUCTION YOU READ INDICATES, THIS ALL
18 COMES DOWN TO THE UNDERSTANDING OF A PERSON OF
19 ORDINARY SKILL.

20 AND CERTAINLY IT'S A FACTUAL ISSUE, BUT
21 IT'S CLEAR TO US THAT AT A VERY MINIMUM THERE'S A
22 MATERIAL DISPUTE OF FACT.

23 AND LET ME STRESS ALSO THAT HYNIX, ON THE
24 VALIDITY ISSUES, HAS THE BURDEN OF PROVING
25 INVALIDITY BY CLEAR AND CONVINCING EVIDENCE, AND

1 THAT, OF COURSE, ALSO IS THE STANDARD TO BE
2 CONSIDERED ON SUMMARY JUDGMENT.

3 THE COURT: BUT LET ME STOP YOU FOR A
4 MINUTE, BECAUSE I THINK THIS IS A DISTINCTION, AT
5 LEAST, THAT I'VE ALWAYS THOUGHT EXISTED -- AND I
6 MAY BE WRONG -- BUT IF YOU'RE TALKING ABOUT
7 SOMETHING LIKE OBVIOUSNESS, YOU'RE TALKING ABOUT
8 WHAT WOULD BE OBVIOUS TO SOMEONE SKILLED IN THE ART
9 FROM READING THIS DISCLOSURE.

10 IN THE WRITTEN DESCRIPTION REQUIREMENT,
11 YOU'RE TRYING TO DETERMINE WHETHER OR NOT THE
12 INVENTOR HAD THAT INVENTION IN MIND AT THE TIME,
13 AND IF IT'S NOT EXPRESSLY SET FORTH, YOU'VE GOT TO
14 SAY THAT SOMEONE READING IT WOULD UNDERSTAND THAT
15 WHATEVER WAS MISSING MUST NECESSARILY BE PRESENT.

16 IN OTHER WORDS, YOU COULDN'T HAVE THE
17 INVENTION WITHOUT IT.

18 MR. DETRE: YES, FROM THE UNDERSTANDING
19 OF A PERSON OF ORDINARY SKILL IN THE ART, AND THE
20 CASES ARE CLEAR THAT THAT'S A FACTUAL ISSUE. IT'S
21 A FACT QUESTION.

22 THE COURT: WELL, NORMALLY IT IS.

23 MR. DETRE: YES.

24 THE COURT: ALL RIGHT.

25 MR. DETRE: AND WHAT I WOULD -- AND I

1 THINK IT'S PRETTY CLEAR, AND IT'S OUR POSITION
2 CERTAINLY THAT IT'S PRETTY CLEAR, THAT A PERSON OF
3 ORDINARY SKILL IN THE ART HERE WOULD UNDERSTAND
4 THAT THERE ARE DISTINCT INVENTIONS, AND WHEN THAT
5 PERSON OF ORDINARY SKILL IS LOOKING AT ONE OF THE
6 INVENTIONS THAT IS NOT RELATED TO THE PACKET, THE
7 PERSON OF ORDINARY SKILL WOULD UNDERSTAND THAT TO
8 UTILIZE THAT INVENTION, YOU NEEDED TO HAVE A READ
9 REQUEST OR AN OPERATION CODE SPECIFYING A READ
10 OPERATION SENT IN SOME FORM. FOR EXAMPLE, FOR THE
11 ACCESS TIME REGISTER, IT WOULDN'T HAVE TO BE IN THE
12 WAY THAT ANOTHER DISTINCT INVENTION SPECIFIED.

13 AND IT CAN'T BE THAT THE UNDERSTANDING OF
14 A PERSON OF ORDINARY SKILL IN THE ART WOULD TURN ON
15 WHETHER SOME, YOU KNOW, ESSENTIALLY BOILER PLATE
16 WAS INCLUDED. "AND BY THE WAY, TO USE AN ACCESS
17 TIME REGISTER, YOU DON'T HAVE TO SEND AN OPERATION
18 CODE IN A PACKET."

19 I THINK A PERSON OF ORDINARY SKILL'S
20 UNDERSTANDING GOES BEYOND THAT AND UNDERSTANDS HOW
21 TO USE DIFFERENT INVENTIONS IN DIFFERENT WAYS.

22 YOU KNOW, THE PATENT SPECIFICATION SHOWS
23 A PARTICULAR KIND OF OUTPUT DRIVER, FOR EXAMPLE.

24 BUT NOBODY WOULD THINK THAT IN ORDER TO
25 USE A PARTICULAR CLOCKING SCHEME DISCLOSED IN THE

1 PATENT OR IN ORDER TO USE AN ACCESS TIME REGISTER
2 OR IN ORDER TO USE THE BLOCK SIZE INFORMATION
3 INVENTION, THAT YOU COULD ONLY USE THOSE WITH THIS
4 PARTICULAR KIND OF OUTPUT DRIVER. THAT'S, THAT'S
5 THE ISSUE AND I THINK IT'S PRETTY CLEAR.

6 I DID WANT TO POINT YOU TO A COUPLE OF
7 THE ORIGINAL CLAIMS. I MENTIONED IN MY ARGUMENT
8 THAT SOME ORIGINAL CLAIMS REFERRED TO A PACKET AND
9 SOME DID NOT.

10 THIS IS -- I WON'T BELABOR THE POINT TOO
11 MUCH. I'LL JUST DIRECT YOUR HONOR TO THE ORIGINAL
12 APPLICATION THAT IS ATTACHED TO MR. BROWN'S
13 DECLARATION IN SUPPORT OF HYNIX'S SUMMARY JUDGMENT
14 MOTIONS. IT'S EXHIBIT 76.

15 AND AT PAGE 103, INTERNAL PAGE NUMBER 103
16 OF THE APPLICATION, WHICH BY HAPPY COINCIDENCE IS
17 ALSO CLAIM 103, WHICH TALKS ABOUT -- IT'S A LENGTHY
18 CLAIM, BUT IN PARTICULAR AT THE END IT TALKS ABOUT
19 RESPONDING TO A REQUEST WHILE, JUST AS ANOTHER
20 EXAMPLE, THERE ARE OTHERS, BUT JUST AS ANOTHER
21 EXAMPLE, CLAIM 24, CLAIM 124, EXCUSE ME, WHICH IS
22 ON PAGE 112 TO 113, TALKS ABOUT RESPONDING TO A
23 REQUEST PACKET.

24 SO THERE IS A DISCLOSURE IN THE ORIGINAL
25 APPLICATION IN ONE CLAIM OF A REQUEST, IN THE OTHER

1 CLAIM OF A REQUEST PACKET, AND I THINK A PERSON OF
2 ORDINARY SKILL IN THE ART WOULD UNDERSTAND THAT THE
3 FORMER IS BROADER THAN THE LATTER.

4 I WOULD ALSO NOTE THAT THERE ARE --
5 MR. BROWN, IN HIS ARGUMENT, SUGGESTED THAT THE
6 WRITTEN DISCLOSURE REALLY HAD TO DISCLOSE EXACTLY
7 WHAT YOU'RE CLAIMING, AND THAT IS SIMPLY NOT THE
8 CASE.

9 AND THERE ARE -- WE CITE VARIOUS CASES --
10 THE COURT: YEAH, I'M PRETTY FAMILIAR
11 WITH THAT.

12 MR. DETRE: OKAY.

13 THE COURT: "IT IS NOT A QUESTION WHETHER
14 ONE SKILLED IN THE ART MIGHT BE ABLE TO CONSTRUCT
15 THE PATENTEE'S DEVICE FROM THE TEACHINGS OF THE
16 DISCLOSURE OF THE APPLICATION. RATHER, IT IS A
17 QUESTION OF WHETHER THE APPLICATION NECESSARILY
18 DISCLOSES THAT PARTICULAR DEVICE."

19 MR. DETRE: OKAY. BUT THERE ARE VARIOUS
20 CASES, AND WE CITE MANY OF THEM IN OUR PAPERS,
21 WHERE THERE'S A CERTAIN DISCLOSURE IN THE PATENT
22 APPLICATION AND BROADER CLAIMS ARE HELD TO BE
23 SUPPORTED BECAUSE OF THE UNDERSTANDING OF A PERSON
24 OF ORDINARY SKILL IN THE ART.

25 ONE EXAMPLE IS THE LAMPI CORP. VERSUS

1 AMERICAN POWER PRODUCTS CASE, 228 F.3D 1365. THE
2 WRITTEN DESCRIPTION ONLY TALKED -- THIS WAS FOR A
3 CERTAIN KIND OF FLORESCENT LIGHT AND THERE WERE TWO
4 HALF SHELLS USED TO CONSTRUCT IT, AND THE WRITTEN
5 DESCRIPTION ONLY TALKED ABOUT IDENTICAL HALF
6 SHELLS, AND THEN, IN FACT, MENTIONED THE ADVANTAGES
7 OF HAVING IDENTICAL HALF SHELLS.

8 AND NEVERTHELESS, THE FEDERAL CIRCUIT
9 HELD THAT CLAIMS THAT HAVE SHELLS THAT WERE NOT
10 IDENTICAL WERE SUPPORTED BY THE WRITTEN
11 DESCRIPTION. A PERSON OF ORDINARY SKILL IN THE ART
12 WOULD UNDERSTAND THAT WHILE YOU MAY WANT IDENTICAL
13 HALF SHELLS FOR CERTAIN REASONS, YOU COULD USE HALF
14 SHELLS THAT WERE NOT IDENTICAL.

15 CORDIS CORP. VERSUS MEDTRONIC, 339 F.3D
16 1352, IN THAT CASE THE PATENT WAS ABOUT A KIND OF A
17 STINT USED IN BALLOON ANGIOPLASTY, AND ALL THAT WAS
18 SHOWN IN THE WRITTEN DESCRIPTION WERE ALTERNATING
19 COMPLETE AND HALF SLOTS AT THE END, AND THE FEDERAL
20 CIRCUIT HELD THAT CLAIMS THAT DID NOT RESTRICT,
21 THAT WERE NOT RESTRICTED IN THAT WAY WERE SUPPORTED
22 BY THE WRITTEN DESCRIPTION.

23 THE COURT: OKAY.

24 MR. DETRE: AND THOSE ARE CASES THAT DO
25 NOT RAISE THE SORT OF DISTINCT INVENTION ISSUE THAT

1 I MENTIONED BEFORE.

2 BUT EVEN IN THOSE CASES, YOU WEREN'T
3 RESTRICTED TO EXACTLY WHAT WAS IN THE WRITTEN
4 DESCRIPTION.

5 THE LAST THING I WANT TO MENTION IN
6 RESPONSE TO WHAT MR. BROWN SAID, MR. BROWN FOCUSED
7 ON THE ORIGINAL RESTRICTION REQUIREMENT AND
8 SUGGESTED THAT THAT SOMEHOW SHOWED THAT ALL OF THE
9 CLAIMS WERE JUST SORT OF SHOWING THESE FEATURES,
10 LIKE THE ACCESS TIME REGISTER, THAT COULD BE USED
11 WITH THE PARTICULAR BUS ARCHITECTURE.

12 AND I WOULD LIKE TO JUST NOTE ANOTHER
13 PART OF THE FEDERAL CIRCUIT OPINION WHERE THEY
14 DISCUSS A LATER RESTRICTION REQUIREMENT, AND I'LL
15 JUST QUOTE FROM THE OPINION.

16 THE FEDERAL -- THIS IS AT PAGE 1095 OF
17 THE FEDERAL CIRCUIT OPINION AFTER DISCUSSING THE
18 ORIGINAL RESTRICTION REQUIREMENT. THE FEDERAL
19 CIRCUIT NOTES, "LATER, DURING PROSECUTION OF THE
20 '580 PATENT," WHICH IT NOTES IS THE GRANDPARENT OF
21 THE '918 PATENT AND THE PARENT OF THE '263 PATENT,
22 "THE PTO ISSUED A TWO-WAY RESTRICTION DIVIDING THE
23 CLAIMS INTO TWO DISTINCT GROUPS, A MULTIPLEXING BUS
24 GROUP, GROUP I, AND A LATENCY INVENTION GROUP,
25 GROUP II. THIS TWO-WAY RESTRICTION STATED, 'THE

1 MEMORY DEVICE IN GROUP I DOES NOT REQUIRE THE
2 ACCESS TIME REGISTER OF GROUP II. AND THE
3 SEMICONDUCTOR DEVICE IN GROUP II DOES NOT REQUIRE
4 THE PLURALITY OF CONDUCTOR BEING MULTIPLEXED TO
5 RECEIVE AN ADDRESS AS CLAIMED IN GROUP I.'"

6 AND THEN THE FEDERAL CIRCUIT GOES ON,
7 "RAMBUS ELECTED TO PROSECUTE THE LATENCY, NAMELY,
8 PROCESS TIME REGISTER, IN THE '580 PATENT,
9 THEREFORE THE CLAIMS OF THE '580 PATENT DO NOT
10 REQUIRE A MULTIPLEXING BUS."

11 SO IT'S PRETTY CLEAR IN THE PTO'S VIEW,
12 AND IN THE FEDERAL CIRCUIT'S VIEW, THAT VARIOUS
13 RAMBUS INVENTIONS, INCLUDING, FOR EXAMPLE, THE
14 ACCESS TIME REGISTER INVENTION AT ISSUE HERE, IS A
15 SEPARATE INVENTION FROM THE BUS.

16 THE COURT: OKAY. YOU WANT TO TALK ABOUT
17 THE CLOCKS?

18 MR. BROWN: I JUST HAVE A COUPLE OF
19 COMMENTS IN RESPONSE TO MR. DETRE.

20 THE COURT: OKAY.

21 MR. BROWN: THERE'S BEEN A LOT OF BACK
22 AND FORTH ABOUT, YOU KNOW, JUST, YOU KNOW, THE
23 INDIVIDUAL PARSING OF WORDS AND PHRASES AND TRYING
24 TO DIVINE INTENT FROM THE FEDERAL CIRCUIT OPINION,
25 AND I CONTINUE TO DISAGREE WITH SOME OF WHAT

1 MR. DETRE SAID, BUT IF IT WOULD BE HELPFUL TO THE
2 COURT, WE COULD SUBMIT SOME ADDITIONAL BRIEFS OR A
3 SHORT BRIEF ON THIS ISSUE ON, YOU KNOW, I -- I JUST
4 DON'T THINK THAT, YOU KNOW, TRYING TO -- THAT
5 SPECULATING ABOUT WHAT ET CETERA MEANS, OR WHAT
6 E.G. MEANS IS A BASIS TO, YOU KNOW -- WOULD BE A
7 FIRM BASIS ON WHICH TO GRANT RAMBUS'S MOTION ON
8 THIS POINT OF READ REQUEST.

9 THE COURT: OKAY.

10 MR. BROWN: OKAY.

11 THE COURT: YOU WANT TO GO TO CLOCKS?

12 MR. BROWN: YES. ACTUALLY, MR. JONES IS
13 GOING TO DO THAT, BUT I HAVE TO SET HIM UP HERE.

14 THE COURT: OKAY.

15 MR. BROWN: I THINK THIS IS IT.

16 MR. JONES: YES.

17 YOUR HONOR, IN LIGHT OF THE TENTATIVE
18 RULING YESTERDAY WITH RESPECT TO THE CONSTRUCTION
19 OF SECOND EXTERNAL CLOCK, I'M REALLY GOING TO FOCUS
20 ON HYNIX'S MOTION FOR NONINFRINGEMENT UNDER HYNIX'S
21 PROPOSED CONSTRUCTION, WHICH IS CONSISTENT, IF NOT
22 IDENTICAL, WITH THE TENTATIVE FROM YESTERDAY.

23 THE "SECOND EXTERNAL CLOCK" TERM IS
24 RECITED IN VARIOUS PATENTS, INCLUDING THE '214, THE
25 '105, THE '365 AND THE '152 PATENTS. THE '214

1 PATENT IS LISTED FIRST AND IS ALSO MENTIONED IN THE
2 PAPERS IN TERMS OF THE, THE PATENT IN WHICH
3 INFINEON WAS GRANTED -- OR THE COURT FOUND FOR
4 INFINEON IN FAVOR OF NONINFRINGEMENT DUE TO A
5 FAILURE OF PROOF ON THE PART OF RAMBUS IN THAT
6 LITIGATION.

7 HOWEVER, MOVING ON TO THE MERITS IN TERMS
8 OF THE CONSTRUCTION PROPOSED BY HYNIX AND THE
9 COURT'S TENTATIVE CONSTRUCTION, THE ONLY ISSUE
10 HERE, AND I'LL MOVE TO THE CONSTRUCTION PROPOSED BY
11 HYNIX, AND THAT WAS, OR IS, "A PERIODIC SIGNAL
12 RECEIVED BY THE MEMORY DEVICE FROM AN EXTERNAL
13 SOURCE TO PROVIDE SECOND TIMING INFORMATION THAT IS
14 DIFFERENT FROM THE FIRST TIMING INFORMATION."

15 IN THIS INSTANCE, THE FIRST TIMING
16 INFORMATION IS PROVIDING REFERENCE TO THE FIRST
17 EXTERNAL CLOCK, AND THE PURPOSE OF THE DEFINITION
18 AS RECITED, EXPLICITLY RECITED, IS THAT THE TWO
19 CLOCKS, THE TWO EXTERNAL CLOCKS ARE PROVIDING
20 DIFFERENT TIMING INFORMATION.

21 NOW, IN TERMS OF THE INFRINGEMENT
22 ALLEGATIONS AGAINST THE ACCUSED HYNIX DOUBLE DATA
23 RATE SDRAM PRODUCTS, DRAM PRODUCTS, RAMBUS IS
24 ESSENTIALLY CONTENDING THAT THE USE OF
25 COMPLEMENTARY CLOCKS THAT ARE FED INTO THE DEVICES

1 EXTERNALLY, AND THAT'S IDENTIFIED HERE AS CK AND CK
2 BAR, ARE ESSENTIALLY TWO EXTERNAL CLOCKS.

3 NOW, UNDER THE DEFINITION THAT'S
4 PROFFERED BY HYNIX AND WHICH WAS REFLECTED IN THE
5 COURT'S TENTATIVE AS OF YESTERDAY, WHAT CAN BE SEEN
6 HERE FROM THIS DIAGRAM IS THE USE OF CLOCK AND
7 CLOCK BAR, IN THIS SENSE THEY ARE COMPLEMENTARY
8 CLOCKS, AND I'LL JUST READ HERE FROM A DATA SHEET
9 OF AN ACCUSED HYNIX DEVICE.

10 AND UP HERE IN THE DESCRIPTION IT SAYS,
11 IT SAYS THAT "CLOCK AND CLOCK BAR ARE DIFFERENTIAL
12 CLOCK INPUTS. ALL ADDRESS AND CONTROL INPUT
13 SIGNALS ARE SAMPLED ON THE CROSSING AND POSITIVE
14 EDGE OF CLOCK AND NEGATIVE EDGE OF CLOCK BAR.
15 OUTPUT," AND THEN PARENTHETICALLY, "(READ DATA IS
16 REFERENCED TO THE CROSSINGS OF CLOCK AND CLOCK
17 BAR)" PARENTHETICALLY, "BOTH DIRECTIONS OF
18 CROSSING."

19 WHAT'S IDENTIFIED HERE WITH THE THREE
20 ARROWS IS REFLECTIVE OF WHAT THAT DESCRIPTION
21 DESCRIBES.

22 THE TIMING INFORMATION PROVIDED BY CLOCK
23 AND CLOCK BAR ARE ESSENTIALLY IDENTICAL. THE
24 DEVICES THAT ARE, THAT ARE RECEIVING THESE CLOCK
25 INPUTS ARE USING THE INFORMATION THAT'S PROVIDED AT

1 THE CROSSING POINTS OF CLOCK AND CLOCK BAR, NOT IN
2 CONTRAST TO WHAT'S DISCLOSED IN THE PREFERRED
3 EMBODIMENT AND THE CLOCKING SCHEME OF THE RAMBUS
4 PATENTS, NOT THE CLOCK EDGES OF ONE VERSUS THE
5 CLOCK EDGES OF ANOTHER TAKEN AT A DIFFERENT TIME,
6 BUT INSTEAD HERE, IDENTICAL TIMING INFORMATION.

7 AND THE QUESTION COULD BE PHRASED LIKE
8 THIS: AT ANY GIVEN TIME, ARE THE CLOCKS PROVIDING
9 DIFFERENT TIMING INFORMATION TO THE DEVICE?

10 AND THE ANSWER TO THAT QUESTION IS NO, AS
11 CAN BE SEEN HERE.

12 WHAT'S HAPPENING IS IT'S -- THE CROSSING
13 POINTS ARE WHERE THE TIMING INFORMATION IS BEING
14 PROVIDED, NOT AT THE RISING EDGE OF ONE THAT'S NOT
15 COINCIDENT WITH THE FALLING EDGE OF ANOTHER CLOCK
16 IN THIS INSTANCE.

17 ONE OF THE ARGUMENTS, OR TWO OF THE
18 ARGUMENTS THAT RAMBUS HAS MADE IS, FIRST, THAT
19 EITHER THE DEVICES WOULD NOT OPERATE WITH JUST ONE
20 OF THESE CLOCKS, OR THE DEVICES WOULD NOT OPERATE
21 AS WELL.

22 AND THE POINT HERE ISN'T THAT, ISN'T THE
23 QUESTION OF WHAT THE PURPOSE OF THE CLOCKS ARE.

24 YES, THE DEVICES OPERATE BETTER WITH
25 COMPLEMENTARY CLOCKS AS OPPOSED TO A SINGLE CLOCK.

1 THE QUESTION IS, DO THE CLOCKS PROVIDE
2 DIFFERENT TIMING INFORMATION?

3 AND FROM THE DEVICE'S PERSPECTIVE, THEY
4 DO NOT, BECAUSE THE DEVICE IS ALWAYS TAKING THE
5 INFORMATION FROM THE CROSSING POINT OF THE RISING
6 EDGE OF ONE CLOCK AND THE FALLING EDGE OF ANOTHER.

7 THE SECOND ARGUMENT THAT RAMBUS MAKES IS
8 THAT, OKAY, THE TIMING DIAGRAMS AND THE CLOCK
9 SIGNALS, THEY'RE REALLY IDEALIZED. THEY'RE NEVER
10 REALLY THIS PERFECT.

11 AND WHAT I'VE DONE HERE IN THIS SLIDE IS
12 JUST KIND OF DEMONSTRATED, OR KIND OF ILLUSTRATED
13 WHAT RAMBUS'S ARGUMENTS ARE.

14 THEIR ARGUMENT ESSENTIALLY BOILS DOWN TO
15 SINCE THESE ARE NOT IDEALIZED, AT CERTAIN POINTS
16 WHERE THAT CROSSING POINT TAKES PLACE, BECAUSE OF
17 THE VARIATIONS IN THE RISE AND FALL TIMES OF THE
18 CLOCKS NOT BEING EXACTLY WHAT'S SHOWN IN THE TIMING
19 DIAGRAMS, YOU KNOW, THERE'S GOING TO BE SOME
20 VARIATION AS TO WHERE THE TWO CLOCK EDGES INTERSECT
21 AND CROSS.

22 THAT DOES NOT REALLY CHANGE THE ISSUE, OR
23 TRANSFORM THE ISSUE IN ANY WAY.

24 WHAT'S STILL HAPPENING IS THAT THE TIMING
25 INFORMATION, REGARDLESS OF WHETHER THERE'S SOME

1 VARIATION FROM THE IDEAL SITUATION, WHICH IS SHOWN
2 IN THE FIRST CROSSING POINT ON THE LEFT, VERSUS THE
3 NON-IDEAL CROSSING POINT, WHICH IS SHOWN AT A LOWER
4 SECTION ON THE, IN THE MIDDLE AND THEN EVEN A
5 HIGHER SECTION ON THE RIGHT, THE FACT REMAINS THE
6 SAME, THAT IT IS THE CROSSING POINTS BETWEEN THOSE
7 TWO SIGNALS WHICH IS PROVIDING THE TIMING
8 INFORMATION. THEY ARE NOT PROVIDING DIFFERENT
9 TIMING INFORMATION.

10 THE CLOCK AND CLOCK BAR ARE ESSENTIALLY
11 MIRROR IMAGES, OR INVERSE IMAGES OF ONE ANOTHER,
12 AND I THINK IT'S HELPFUL TO ACTUALLY LOOK AT THE
13 CLOCKING SCHEME AT LEAST TO GIVE CONTEXT TO THIS,
14 LOOK AT THE CLOCKING SCHEME THAT'S DISCLOSED IN THE
15 PREFERRED EMBODIMENT OF THE RAMBUS PATENT.

16 FIGURE 8 OF THE PATENTS, AGAIN, THIS WAS
17 ADDRESSED YESTERDAY AND I THINK EVEN IN THE
18 TUTORIAL ON THURSDAY, SHOWS THE ONE AND ONLY
19 CLOCKING SCHEME DISCLOSED IN THE PATENTS, AND
20 THAT'S SHOWING CLOCK LINE 53, LOOPING CLOCK 1 OUT
21 FROM THE CLOCK GENERATOR, AND THEN ONCE THAT CLOCK
22 RETURNS ALONG THE U, IT'S FED AGAIN INTO THE TWO
23 CHIPS THAT ARE CONNECTED, OR TWO DEVICES THAT ARE
24 CONNECTED TO THE CLOCK BUS LINE.

25 NOW, WHAT'S INTERESTING ABOUT THAT IS IN

1 CONTRAST TO COMPLEMENTARY CLOCKS, THE ORDER IN
2 WHICH THOSE CLOCKS ARE RECEIVED AT THOSE TWO
3 DEVICES IS PROVIDING DIFFERENT TIMING INFORMATION.

4 FOR EXAMPLE, THE FIRST CHIP IN THIS
5 INSTANCE, IT'S GOING TO BE CHIP 0, WILL RECEIVE
6 CLOCK NUMBER 1 PRIOR TO CHIP N RECEIVING ANY
7 INFORMATION, AND THAT'S PROVIDING A FIRST TIMING
8 INFORMATION.

9 THEN THE NEXT THING THAT HAPPENS, AT
10 LEAST IN FIGURE 8A THAT WAS SHOWN BEFORE, IS THAT
11 IN SEQUENCE OF TIME, THE FIRST CLOCK EDGE IS NOW
12 GOING TO REACH THE SECOND CHIP BECAUSE IT'S ON THE
13 -- WHAT'S HAPPENING HERE IS THE FIRST CLOCK, CLOCK
14 1, IS GOING TO BE SAMPLED AND PROVIDE A TIMING
15 INFORMATION TO CHIP 0.

16 THAT CLOCK PULSE IS GOING TO CONTINUE
17 ALONG THE CLOCK BUS LINE 53 AND THEN BE RECEIVED AT
18 CHIP N.

19 NOW, CLOCK 2 IS THE SAME SIGNAL ONCE IT'S
20 TURNED AROUND AT THE U POINT.

21 NOW, RETURNING BACK TO THE DIAGRAM I WAS
22 SHOWING, CLOCK 1 GETS RECEIVED AT CHIP 0, THEN IT
23 GETS RECEIVED AT CHIP N.

24 NOW, ONCE THE CLOCK SIGNAL HAS MADE ITS
25 WAY AROUND THE U, IT'S GOING TO BE SAMPLED THIS

1 TIME AT CHIP N, AND IN THIS INSTANCE IT'S CALLED
2 CLOCK 2, OR THE LATE CLOCK.

3 THEN FINALLY AS IT MAKES ITS WAY AROUND
4 THE U, IT'S GOING TO BE RECEIVED AT CHIP O, WHICH
5 WAS THE CHIP THAT WAS CLOSEST TO THE CLOCK
6 GENERATOR IN THE PRIOR EXAMPLE.

7 NOW, WHAT CAN BE SEEN HERE IS THAT BOTH
8 OF THESE CHIPS ARE RECEIVING TWO EXTERNAL CLOCKS,
9 CLOCK 1 AND CLOCK 2, AND THEY'RE SAMPLING BOTH
10 CLOCK 1, THE RISING EDGES OF BOTH CLOCK 1 AND CLOCK
11 2.

12 THEY'RE DOING THIS IN ORDER TO CORRECT
13 FOR SKEW SO THAT THE, OR CLOCK SKEW SO THAT THE
14 DEVICES THAT ARE ATTACHED TO THE BUS, NO MATTER
15 WHERE THEY ARE, WILL BE ABLE TO OPERATE IN SYNC
16 WITH ONE ANOTHER.

17 AND THE WAY THAT'S DONE IS IF YOU LOOK AT
18 THE DOTTED LINE EXTENDING VERTICALLY ABOVE 59,
19 ESSENTIALLY THE CLOCKING SCHEME TAKES THE TWO
20 TIMING INFORMATIONS PROVIDED BY CLOCK 1 AND CLOCK 2
21 AND IT DERIVES THE MID-POINT, AND THAT MID-POINT,
22 AS REFLECTED IN THIS DIAGRAM, THE MID-POINT FOR
23 EACH OF THE DEVICES IS GOING TO BE THE SAME SO THAT
24 OFF OF THAT MID-POINT FROM THOSE TWO CLOCKS, AN
25 INTERNAL CLOCK CAN BE DERIVED.

1 BUT THE IMPORTANT THING IN NOTING THIS,
2 AND THIS IS WHY THE DEFINITION THAT'S BEEN
3 PROFFERED BY HYNIX IS THE ONE WHICH WE THINK IS
4 CORRECT, IS THAT THE INFORMATION THAT'S BEING
5 RECEIVED FROM EACH OF THOSE CLOCKS IS DIFFERENT
6 TIMING INFORMATION.

7 WITH RESPECT TO JUST THE CHIP 0 ON THE
8 BOTTOM, CLOCK 1 IS RECEIVED FIRST, AND THEN SOME
9 TIME LATER IT'S GETTING INFORMATION, A DIFFERENT
10 TIMING INFORMATION, FROM CLOCK 2.

11 IN CONTRAST, IN THE ACCUSED HYNIX
12 DEVICES, THE TIMING INFORMATION IS ONLY BEING
13 PROVIDED WHERE THE TWO CLOCKS CROSS, AND IT DOESN'T
14 MATTER THAT THAT CROSSING POINT MIGHT VARY OR
15 FLUCTUATE FROM WHAT'S IDEAL.

16 THE POINT IS THAT AT EACH INSTANCE WHERE
17 THE CLOCKS ARE BEING SAMPLED, THEY'RE BEING SAMPLED
18 TOGETHER AND THERE'S IDENTICAL TIMING INFORMATION.

19 IT'S NOT SAMPLING TWO DIFFERENT CLOCKS AT
20 TWO DIFFERENT TIMES. IT'S NOT SAMPLING OR LOOKING
21 AT THE COMPLEMENTARY CLOCKS.

22 IF I CAN BACK UP HERE, IT'S NOT LOOKING
23 AT, FOR EXAMPLE, IF WE WERE TO LOOK AT, MOVE ONE OF
24 THESE ARROWS TO THE RIGHT WHERE CLOCK BAR, WHICH IS
25 DEPICTED IN DOTTED GREEN LINE, IS LOW AND WHERE

1 CLOCK IS HIGH, WHICH IS BLUE, THE DEVICES THAT ARE
2 ACCUSED OF INFRINGEMENT HERE ARE NOT SAMPLING
3 INFORMATION AND TAKING THE SIGNALS FROM THOSE
4 CLOCKS AT ANY OTHER POINT OTHER THAN THE CROSSING
5 POINTS.

6 NOW, IF THE CLOCKS BEING SAMPLED IN THE
7 MIDDLE OF THOSE SIGNALS ARE CLOCK WAS HIGH AND
8 CLOCK BAR WAS LOW, THAT WOULD POTENTIALLY BE
9 PROVIDING A DIFFERENT TIMING INFORMATION BECAUSE AT
10 THAT POINT ONE IS A LOGIC HIGH AND ONE IS A LOGIC
11 LOW.

12 BUT WHAT, IN FACT, IS GOING ON IS IT'S
13 THE TWO INFORMATION AT THE CROSSING POINTS THAT ARE
14 PROVIDING THE CLOCK INFORMATION, OR I SHOULD SAY
15 THE IDENTICAL TIMING INFORMATION.

16 THE COURT: AREN'T YOU, IN ESSENCE,
17 THOUGH, WHEN YOU PICK THE CROSSING POINT, COMPARING
18 CLOCK 1 AND CLOCK 2?

19 MR. JONES: YES, THEY ARE BEING COMPARED,
20 YES.

21 BUT THEY'RE STILL PROVIDING THE SAME
22 INFORMATION. I MEAN, IT'S, IN ESSENCE, INSTEAD OF
23 READING JUST THE FALLING EDGE OF ONE CLOCK, OR JUST
24 THE RISING EDGE OF ONE CLOCK TO DENOTE YOUR TIMING
25 INFORMATION, OR IN CONTRAST TO WHAT RAMBUS IS

1 DOING, LOOKING AT THE RISING EDGE OF ONE CLOCK AND
2 THE FALLING EDGE, OR THE RISING EDGE OF ANOTHER
3 CLOCK AT ANOTHER TIME, THIS TIMING INFORMATION IS
4 ALWAYS THE CROSSING POINT.

5 THE COURT: I UNDERSTAND THAT, AND I SEE
6 HOW IT'S QUITE DIFFERENT IN SOME WAYS THAN
7 RAMBUS'S.

8 BUT IT IS COMPARING TWO CLOCKS, THE
9 RISING ON ONE AND THE GOING DOWN ON THE OTHER, AND
10 COMPARING THEM TO FIND OUT WHERE THEY CROSS.

11 MR. JONES: WELL, I THINK, YOUR HONOR,
12 WHAT'S HAPPENING -- WELL, THAT IS A WAY TO
13 CHARACTERIZE IT.

14 BUT WHAT'S HAPPENING IS THE INFORMATION
15 THAT'S BEING DERIVED FROM THE SIGNALS IS ALWAYS
16 BEING DERIVED AT THAT CROSSING POINT.

17 THE COURT: RIGHT.

18 MR. JONES: AND THAT'S ONE BIT OF
19 INFORMATION AT THAT PARTICULAR TIME IN CROSSING,
20 AND THAT'S THE TIMING INFORMATION.

21 IF WE WERE TO SAMPLE THE CLOCKS AT ANY
22 OTHER POINT IN TIME TO DERIVE TIMING INFORMATION,
23 THEN THEY WOULD BE PROVIDING DIFFERENT TIMING
24 INFORMATION.

25 IF WE WERE GOING TO LOOK AT --

1 THE COURT: SO IF WE SAMPLED AT THE PEAK,
2 AT THE TOP AND THE BOTTOM AND TOOK AN AVERAGE, THAT
3 WOULD BE SAMPLING THAT WOULD MEET THE LIMITATION?

4 MR. JONES: I'M NOT SURE I'M FOLLOWING.

5 I GUESS WHAT I'M SAYING IS IF YOUR
6 REFERENCE POINT IS WHETHER YOUR CLOCKS ARE HIGH OR
7 LOW AND YOU WERE TO SAMPLE -- AND YOUR CRITERIA
8 WAS, WELL, I WANT TO KNOW AT A GIVEN PARTICULAR
9 TIME, IS THE CLOCK HIGH, IS ONE CLOCK HIGH AND IS
10 ONE CLOCK LOW AND WHERE THOSE POINTS IN TIME ARE,
11 THEN, YES, THAT WOULD PROBABLY MEET THE LIMITATION.

12 THE COURT: IN OTHER WORDS, IF YOU SAMPLE
13 ANYWHERE OTHER THAN THE CROSSING POINT?

14 MR. JONES: YES, I -- WELL, NOT
15 NECESSARILY, YOUR HONOR.

16 I GUESS THE OTHER THING TO EMPHASIZE IS
17 THAT ALTHOUGH THEY ARE IDEALIZED, THEY'RE
18 ESSENTIALLY MIRROR IMAGES OF ONE ANOTHER, INVERSES,
19 SO THAT THE -- IN THE IDEAL SITUATION, THE RISING
20 EDGE OF ONE CLOCK IS GOING TO BEGIN WHEN THE
21 FALLING EDGE OF ANOTHER ONE ALSO TAKES PLACE.

22 SO IF YOU WERE TO LOOK AT THAT PARTICULAR
23 POINT IN TIME, THE INFORMATION, IT'S JUST OF MATTER
24 OF WHETHER YOU'RE SEEING A LOGICAL HIGH OR A
25 LOGICAL LOW.

1 NOW, THE REASON THE CROSSING POINT IS
2 TAKEN IS BECAUSE PROBABLY, IN PART, ALTHOUGH I --
3 THIS IS IDEALIZED. IT'S NOT NECESSARILY THE BEST
4 PLACE TO SAMPLE THE CLOCK SIGNALS.

5 AND SO IF YOU TAKE THE CLOCK AND USE, AS
6 YOUR REFERENCE POINT, THE CROSSING POINT, THAT
7 PROVIDES A MORE EFFECTIVE WAY OF, OF TIMING THE
8 CLOCK.

9 IF YOU IMAGINE, FOR ONCE, IF YOU TOOK
10 AWAY, IN THIS EXAMPLE, CLOCK BAR, WHICH IS
11 IDENTIFIED WITH THE DOTTED GREEN LINES, YOUR OPTION
12 HERE, AND REALLY THIS IS NO DIFFERENT, IS THAT YOU
13 WOULD BE SAMPLING -- INSTEAD OF SAMPLING AT THE
14 CROSSING POINT, YOU'RE ESSENTIALLY SAMPLING AT THE
15 RISING EDGE OF CLOCK ON EVERY PULSE, OR THE RISING
16 EDGE OF CLOCK HERE, AND IN THE MIDDLE YOU'RE
17 SAMPLING THE FALLING EDGE OF CLOCK, AND IN THE LAST
18 EXAMPLE YOU'RE SAMPLING THE RISING EDGE OF CLOCK.

19 NOW, THE ADDITION OF CLOCK BAR MAY
20 PROVIDE FOR ADDITIONAL AND MORE PRECISE TIMING.

21 BUT THE INFORMATION AND THE POINTS AT
22 WHICH THAT INFORMATION IS BEING TAKEN, THAT TIMING
23 INFORMATION, HAS NOT CHANGED.

24 THE COURT: OKAY. ALL RIGHT.

25 MR. DETRE: YOUR HONOR, I THINK THAT

1 HYNIX IS REALLY MUDDLING TOGETHER TWO DIFFERENT
2 POINTS HERE, AND I DON'T THINK EITHER POINT REALLY
3 HOLDS UP.

4 AND ONE POINT SEEMS TO BE THAT THEIR
5 COMPLEMENTARY CLOCKS DON'T PROVIDE DIFFERENT TIMING
6 INFORMATION BECAUSE THEY'RE JUST PROVIDING A SINGLE
7 TIMING REFERENCE TO THE DEVICE AT THE CROSSING
8 POINT.

9 THE OTHER POINT SEEMS TO BE THAT THEY'VE
10 GOT THESE COMPLEMENTARY CLOCKS THAT ARE JUST MIRROR
11 IMAGES OF ONE ANOTHER AND THAT MEANS THEY DON'T
12 PROVIDE DIFFERENT TIMING INFORMATION.

13 SO I'D LIKE TO TAKE THOSE IN ORDER.

14 WITH RESPECT TO THE FIRST POINT, THAT
15 BECAUSE YOU'RE TAKING THESE TWO DIFFERENT CLOCK
16 SIGNALS, THEY ARE DIFFERENT, ONE -- EVEN IF THEY
17 WERE PERFECTLY COMPLEMENTARY, ONE HAS THE RISING
18 EDGE AND THE OTHER HAS THE FALLING EDGE AND THAT'S
19 WHAT ENABLES YOU TO FIND THE CROSSING POINT.

20 IF THEY WERE IDENTICAL CLOCK SIGNALS, OF
21 COURSE, YOU COULD NOT FIND THE CROSSING POINT.

22 THEY -- THIS IS ESSENTIALLY WHAT GOES ON
23 IN THE RAMBUS PREFERRED EMBODIMENT THAT MR. JONES
24 WAS DOING HIS BEST TO DISTINGUISH.

25 IT'S TRUE THAT THE RAMBUS PREFERRED

1 EMBODIMENT TAKES TWO DIFFERENT CLOCK SIGNALS AND
2 FINDS THE MID-POINT, WHICH IT THEN USES AS A TIMING
3 REFERENCE.

4 THE HYNIX DEVICES TAKE TWO DIFFERENT
5 CLOCK SIGNALS AND FINDS THE CROSSING POINT AND USES
6 THAT AS THE TIMING REFERENCE.

7 IN BOTH CASES, YOU TAKE TWO DIFFERENT
8 CLOCK SIGNALS PROVIDING DIFFERENT INFORMATION AND
9 COMBINE THEM IN ORDER TO PROVIDE A TIMING REFERENCE
10 TO THE DEVICE.

11 THAT'S HYNIX'S FIRST POINT.

12 THE OTHER POINT SEEMS TO BE THAT
13 COMPLEMENTARY CLOCKS DON'T REALLY PROVIDE DIFFERENT
14 TIMING INFORMATION BECAUSE THEY'RE JUST MIRROR
15 IMAGES.

16 AS I MENTIONED, THEY DO PROVIDE DIFFERENT
17 TIMING INFORMATION. THAT'S WHAT ALLOWS YOU TO FIND
18 THE CROSSING POINT.

19 THE SECOND POINT, IT'S CERTAINLY NOT THE
20 CASE THAT COMPLEMENTARY CLOCKS IN THE ABSTRACT
21 DON'T PROVIDE DIFFERENT TIMING INFORMATION.

22 AS YOU MAY RECALL FROM THE DISCUSSION
23 YESTERDAY, RAMBUS'S EMBODIMENT ALSO HAS TWO
24 INTERNAL CLOCKS WHICH ARE COMPLEMENTS OF ONE
25 ANOTHER.

1 AND YOU MAY RECALL MR. JONES SAYING
2 YESTERDAY, WELL, HYNIX AGREED TO THE CONSTRUCTION
3 OF INTERNAL CLOCKS WITHOUT THE DIFFERENT TIMING
4 INFORMATION LIMITATION BECAUSE THOSE TWO CLOCKS ARE
5 JUST COMPLEMENTS OF ONE ANOTHER, THEY DON'T PROVIDE
6 DIFFERENT TIMING INFORMATION.

7 HYNIX'S EXPERT, HOWEVER, IS OF A
8 DIFFERENT VIEW. MR. TAYLOR, IN HIS DEPOSITION --
9 WE DISCUSSED THOSE INTERNAL CLOCKS AND THAT THEY
10 WERE COMPLEMENTS OF ONE ANOTHER IN THE RAMBUS
11 PREFERRED EMBODIMENT.

12 AND THEN I ASKED MR. TAYLOR, THIS IS ON
13 PAGE 51 OF HIS DEPOSITION AT LINE 20, "OKAY. SO
14 THAT -- IS IT FAIR TO SAY, THEN, THAT THE TWO
15 INTERNAL CLOCKS IN THE RAMBUS PREFERRED EMBODIMENT,
16 WHEN YOU CONSIDER THEM IN CONNECTION WITH THE
17 OUTPUTTING OF DATA, PROVIDE DIFFERENT TIMING
18 INFORMATION?"

19 AND MR. TAYLOR ANSWERED, "YES."

20 SO THERE'S AN EXAMPLE OF TWO
21 COMPLEMENTARY CLOCKS THAT HYNIX APPARENTLY AGREES
22 PROVIDE DIFFERENT TIMING INFORMATION.

23 THE THIRD POINT I WANT TO MAKE IS,
24 RELATES TO THIS IDEA THAT, IN FACT, CLOCKS, IN
25 PRACTICE, WILL NOT BE PERFECTLY COMPLEMENTARY.

1 HYNIX'S DATA SHEET PROVIDES FOR A MARGIN.
2 IF THE CLOCKS WERE PERFECTLY COMPLEMENTARY, THE
3 CROSSING POINT WILL ALWAYS APPEAR ON THAT
4 MID-VOLTAGE LINE AS SHOWN IN MR. JONES' GRAPHIC.

5 IN HYNIX'S DATA SHEETS, IT PROVIDES FOR A
6 MARGIN OF PLUS OR MINUS TWO VOLTS WHERE THAT
7 CROSSING POINT CAN APPEAR AND STILL SATISFY THE
8 REQUIREMENTS OF THE DEVICE.

9 NOW, IF WE COULD PULL UP THAT MICRON
10 TECHNICAL NOTE, AND GO TO THE -- TO THAT PAGE. AND
11 CAN WE BLOW UP THE FIGURE?

12 THIS IS ACTUALLY A FIGURE FROM A MICRON
13 TECHNICAL NOTE, BUT I JUST WANT TO USE IT FOR
14 ILLUSTRATIVE PURPOSES.

15 I SHOWED THIS TO MR. TAYLOR AT HIS
16 DEPOSITION AND HE AGREED THAT THIS BASICALLY
17 ILLUSTRATED THAT POINT OF THE MARGIN THAT YOU COULD
18 HAVE WHERE THE CROSSING POINTS ACTUALLY ARE, FOR
19 NON-IDEALIZED CLOCKS, AND THEY COULD -- HERE'S A
20 CROSSING POINT THAT'S .2 VOLTS BELOW THE MID-LINE.

21 THE COURT: OKAY. I UNDERSTAND THAT.

22 MR. DETRE: OKAY. AND AS MR. JONES
23 MENTIONED, HYNIX USES THESE MORE OR LESS
24 COMPLEMENTARY CLOCKS IN ORDER TO ACHIEVE MORE
25 PRECISE TIMING.

1 THE REASON THAT YOU GET MORE PRECISE
2 TIMING IS PRECISELY IN THIS SITUATION WHERE THE
3 CLOCKS DON'T CROSS RIGHT AT THE MID-POINT VOLTAGE.

4 IF THE CLOCKS WERE CROSSING RIGHT AT THE
5 MID-POINT VOLTAGE, YOU COULD HAVE A SINGLE CLOCK IN
6 THAT MID-LINE VOLTAGE REFERENCE AND GET THE EXACT
7 SAME POINT.

8 BUT HERE IF YOU USE A SINGLE CLOCK IN THE
9 MID-LINE VOLTAGE REFERENCE WHERE THE CLOCKS ARE NOT
10 PERFECT, USING THIS CROSSING POINT OF THE
11 DIFFERENTIAL CLOCKS, OF THE DIFFERENTIAL CLOCK, OR
12 THE MORE OR LESS COMPLEMENTARY CLOCK SIGNALS ALLOWS
13 FOR A MORE PRECISE, A MORE REGULAR TIMING
14 REFERENCE.

15 THE COURT: ISN'T THE ESSENTIAL
16 DIFFERENCE BETWEEN YOUR SET UP AND HYNIX'S IS THAT
17 YOU DO YOUR TIMING MEASUREMENTS AT DIFFERENT POINTS
18 IN TIME, WHERE HYNIX DOES IT AT THE SAME TIME?

19 MR. DETRE: I DON'T THINK SO.

20 OH, I SEE. IN HYNIX'S DEVICES, HYNIX'S
21 DEVICES RECEIVE THE COMPLEMENTARY --

22 THE COURT: RIGHT.

23 MR. DETRE: -- CLOCKS AT ESSENTIALLY THE
24 SAME TIME AND THEN CALCULATE THE CROSSING POINT,
25 AND THE RAMBUS PREFERRED EMBODIMENT RECEIVES THE

1 EARLY AND LATE CLOCKS --

2 THE COURT: RIGHT.

3 MR. DETRE: -- AT -- WELL, I -- I MEAN, I
4 THINK IN EACH CASE THE -- I MEAN, THESE ARE
5 CONTINUOUS CLOCK SIGNALS THAT ARE BEING SUPPLIED TO
6 THE DEVICE.

7 IN EACH CASE IN THE RAMBUS PREFERRED
8 EMBODIMENT, THE DEVICES ARE RECEIVING THIS EARLY
9 CLOCK, IT'S A CLOCK SIGNAL GOING UP AND DOWN, AND
10 THEY'RE RECEIVING THE LATE CLOCK AND CALCULATING
11 THAT MID-POINT.

12 IN THE HYNIX DEVICES, THEY'RE RECEIVING
13 THE, THE TWO COMPLEMENTARY CLOCK SIGNALS
14 CONTINUOUSLY IN THE SAME WAY AND CALCULATING THE
15 CROSS POINTS, SO I DON'T THINK THAT THAT'S REALLY A
16 DISTINCTION.

17 FINALLY, THE LAST POINT I WANT TO MAKE
18 ABOUT THIS IS THAT, IN FACT, THE PREFERRED
19 EMBODIMENT IN THE RAMBUS PATENT ALSO INCLUDES, AS A
20 SPECIAL CASE, THE SITUATION WHERE THAT EARLY AND
21 LATE CLOCK WILL, IN FACT, BE COMPLEMENTS OF ONE
22 ANOTHER.

23 AND THAT'S BECAUSE THE EARLY CLOCK COMES
24 IN, THE LATE CLOCK COMES IN AT SOME POINT LATER,
25 PHASE SHIFTED, AND IF IT'S PHASE SHIFTED BY JUST

1 THE RIGHT AMOUNT, THEN THE RISING EDGE OF THE EARLY
2 CLOCK WILL LINE UP WITH THE FALLING EDGE OF THE
3 LATE CLOCK AND THERE WILL BE COMPLEMENTARY CLOCK
4 SIGNALS COMING IN.

5 HYNIX, IN ITS -- WE POINTED THIS OUT AND
6 HYNIX RESPONDED, WELL, YOU KNOW, THIS IS JUST SOME
7 MADE UP EXAMPLE ON RAMBUS'S PART BECAUSE IN THAT
8 CASE THERE WOULD BE EXCESSIVE DELAY AND IT'S NOT
9 REALLY A SITUATION CONTEMPLATED BY THE PATENT.

10 THE COURT: RIGHT.

11 MR. DETRE: AND I DISAGREE WITH THAT AND
12 I'D LIKE TO EXPLAIN WHY.

13 IF WE COULD GO TO THE '263 PATENT AT PAGE
14 25. COLUMN 17, RIGHT AT THE BOTTOM. BLOW IT UP.
15 THAT'S FINE. WHERE YOU WERE BEFORE, THAT'S FINE.
16 EITHER WAY.

17 AND THIS IS TALKING ABOUT, IN THE
18 PREFERRED EMBODIMENT, WHAT THE -- YOU WANT TO KEEP
19 THE BUS SHORT IN THE RAMBUS PREFERRED EMBODIMENT
20 BECAUSE THAT'S WHAT ALLOWS FOR HIGH-SPEED
21 COMMUNICATION WITHOUT TOO MUCH OF A TIME LAG AMONG
22 DEVICES.

23 AND YOU'VE GOT A 500 MEGAHERTZ CLOCK IN
24 THE PREFERRED EMBODIMENT WHICH, AS THE
25 SPECIFICATION NOTES HERE, CORRESPONDS TO TWO

1 NANOSECOND BUS CYCLES, FOUR NANOSECOND BUS CYCLES,
2 AND THERE ARE TWO BUS CYCLES PER CLOCK CYCLE.

3 AND THEN IT POINTS OUT, "TO OPERATE AT A
4 TWO NANOSECOND DATA RATE," I'M READING AT LINE 63,
5 "THE TRANSIT TIME ON THE BUS SHOULD PREFERABLY BE
6 KEPT UNDER ONE NANOSECOND TO LEAVE ONE NANOSECOND
7 FOR THE SETUP AND HOLD TIME OF THE INPUT
8 RECEIVERS."

9 IF WE -- LET'S GO UP TO THE TOP OF THE
10 NEXT COLUMN, COLUMN 18. JUST THAT, YEAH, VERY
11 LITTLE BIT. THERE WE GO.

12 IT NOTES THAT YOU CAN HAVE LOWER
13 PERFORMANCE SYSTEMS WITH LONGER LINES, BUT IN THE
14 VERY PREFERRED EMBODIMENT, YOU WANT TO KEEP THAT
15 BUS TRANSIT TIME DOWN TO ONE NANOSECOND.

16 SO I'D LIKE TO JUST BRIEFLY DISCUSS WHAT
17 THAT MEANS ABOUT WHERE THE EARLY CLOCKS AND THE
18 LATE CLOCKS SHOW UP.

19 COULD WE GO TO GRAPHIC NUMBER 67?

20 AND THIS IS JUST A FIGURE FROM THE PATENT
21 THAT WE'VE MODIFIED SLIGHTLY. I THINK IT'S FIGURE
22 2. YEAH, IT'S FIGURE 2 SHOWING, SHOWING THE
23 PREFERRED EMBODIMENT OF THE BUS.

24 AND WE'VE JUST -- WE'RE ASSUMING, IT'S
25 NOT NECESSARILY THE CASE, BUT WE'RE ASSUMING FOR

1 THIS EXAMPLE THAT THE CLOCK, CLOCK 1 AND CLOCK 2 AS
2 SHOWN IN THIS PREFERRED EMBODIMENT, GO ALONG BUS
3 LINES OF ESSENTIALLY THE SAME LENGTH AS THE REST OF
4 THE BUS.

5 AND WE'VE MODIFIED THE FIGURE TO PUT IN
6 THAT CLOCK LOOP AT THE LEFT-HAND SIDE OF CLOCK 1
7 AND CLOCK 2.

8 NOW, IN THE PREFERRED LENGTH OF THE BUS
9 DESCRIBED IN THE PATENT SPECIFICATION I JUST READ,
10 IT'S THE TRANSIT TIME ON THE BUS, AND THAT'S
11 BETWEEN DEVICES. THAT'S ONE-WAY TRANSIT TIME THAT
12 SHOULD BE KEPT TO ONE NANOSECOND.

13 THAT MEANS THAT THE CLOCK LOOP TRANSIT
14 TIME THAT THE CLOCK GOES FROM ONE AND THEN LOOPS
15 BACK AROUND IS TWO NANoseconds.

16 IN THE PREFERRED EMBODIMENT WE'VE GOT A
17 250 MEGAHERTZ CLOCK, AND THAT CORRESPONDS AS SHOWN
18 IN THE BOTTOM, WE'VE ADDED THIS TO THE FIGURE, A
19 FOUR NANOSECOND PERIOD, A FOUR NANOSECOND CYCLE
20 TIME.

21 AND IF YOU'VE GOT IN THIS, IN WHAT'S
22 DESCRIBED AS THE PREFERRED LENGTH OF THE BUS IN THE
23 PATENT SPECIFICATION, IF YOU'VE GOT DEVICES
24 PRECISELY AT ONE END GETTING THE EARLY CLOCK AS
25 EARLY AS CAN BE, AND AT THE OTHER END GETTING THE

1 LATE CLOCK AS LATE AS CAN BE, YOU'VE SHIFTED, BY
2 TWO NANoseconds PRECISELY. THAT'S THE CLOCK LOOP
3 TRANSIT TIME.

4 AND YOU MOVE THAT CLOCK OVER BY TWO
5 NANoseconds AND YOU'VE GOT YOUR COMPLEMENTARY
6 CLOCKS.

7 SO NOTHING MADE UP ABOUT THAT EXAMPLE.
8 IT'S A PRECISE KIND OF EXAMPLE THAT YOU CAN HAVE IF
9 YOU FOLLOW THE INSTRUCTIONS IN THE PATENT FOR THE
10 VERY PREFERRED EMBODIMENT.

11 THAT'S ALL I HAVE TO SAY ABOUT THIS
12 ISSUE.

13 THE COURT: OKAY. DO YOU HAVE ANYTHING
14 FURTHER ON THAT? YOU DON'T NEED TO, I JUST --

15 MR. JONES: WELL, SOMETIMES YOU FEEL
16 COMPELLED TO.

17 BUT THE -- YOU KNOW, THERE ARE TWO MAKE
18 BELIEVE, OR CONCOCTED POSSIBILITIES FROM THE RAMBUS
19 PERSPECTIVE WHEN THEY TALK ABOUT WHAT COULD BE, AND
20 ONE MR. DETRE JUST SPOKE ABOUT, WHICH IS IF YOU
21 MAKE THE BUS LONG ENOUGH AND ONE CHIP THAT'S CLOSE
22 ENOUGH TO THE CLOCK GENERATOR SUCH THAT BY THE TIME
23 THE EARLY CLOCK BECOMES THE LATE CLOCK, THAT ONE
24 CHIP IS GOING TO SEE A COMPLEMENTARY CLOCK.

25 THE OTHER ONE, WHICH WASN'T SUGGESTED

1 TODAY, OR AT LEAST WASN'T MENTIONED IN THE LAST FEW
2 MOMENTS, WAS -- AND THEN THE OTHER INSTANCE IS,
3 OKAY, WHAT IF YOU TOOK ONE OF THESE DEVICES AND YOU
4 PUT IT AT THE U-TURN OF THE CLOCK SO THAT AT THAT
5 POINT CLOCK 1 AND CLOCK 2 ARE PROVIDING THE SAME
6 INFORMATION?

7 NOW, THIS KIND OF DOVETAILS INTO WHY
8 HYNIX PROFFERED THE CONSTRUCTION IT DID, AND THE
9 ALTERNATE ARGUMENTS THAT HAVE BEEN PRESENTED IN OUR
10 MOTION, OR ALTERNATE GROUNDS, AS TO WHY YOU NEED
11 TWO DIFFERENT TIMING INFORMATIONS PROVIDED BY THESE
12 CLOCKS, AND THAT IS THAT THOSE TWO MAKE UP, MADE UP
13 OR CONCOCTED HYPOTHETICALS ARE NOT DISCLOSED WITHIN
14 THE SPECIFICATION.

15 THERE'S NO SUGGESTION THAT RECEIVING BOTH
16 CLOCKS AT THE SAME TIME AND HAVING THEM
17 COMPLEMENTARY, IN FACT, ACCOUNTS FOR HAVING TWO
18 EXTERNAL CLOCKS PROVIDING TWO DIFFERENT TIMING
19 INFORMATIONS.

20 AND THE POSSIBILITY OF PUTTING ONE AT THE
21 END AND ONE AT THE U-TURN IS NOWHERE WITHIN THE
22 SPECIFICATION, NOR WITHIN THE FILE HISTORY, AND
23 NOWHERE EVEN WITHIN THE CLAIMS AS ORIGINALLY FILED.

24 THE COURT: ALL RIGHT.

25 YOU WANTED TO MENTION SOMETHING ABOUT

1 SYNCHRONOUS MEMORY DEVICE?

2 MR. DETRE: YES, YOUR HONOR, AND I'LL BE
3 BRIEF BECAUSE I -- IT IS FAIRLY WELL LAID OUT IN
4 OUR PAPERS, BUT THERE ARE A COUPLE OF POINTS I'D
5 LIKE TO STRESS, ONE OF WHICH IS NOT EXPRESSLY IN
6 OUR PAPERS.

7 ON SYNCHRONOUS MEMORY DEVICE, HYNIX
8 ARGUES ESSENTIALLY THAT ALL OF RAMBUS'S CLAIMS
9 INVOLVING SYNCHRONOUS MEMORY DEVICE NEED TO BE
10 RESTRICTED TO THE PREFERRED CLOCK DISTRIBUTION
11 SCHEME THAT WE'VE BEEN DISCUSSING, THE EARLY CLOCK
12 AND A LATE CLOCK AND CALCULATING THE MID-POINT IS
13 ESSENTIALLY THE USUAL ARGUMENT BECAUSE THEY SAY
14 THAT'S THE ONLY TYPE OF CLOCK DISTRIBUTION SCHEME
15 DESCRIBED IN THE PATENTS.

16 I WANT TO MAKE THE POINT -- TO SOME
17 EXTENT, THIS OVERLAPS OUR OTHER ARGUMENTS THAT A
18 PERSON OF ORDINARY SKILL WOULD UNDERSTAND THAT
19 DISTINCT INVENTIONS COULD BE USED WITH OTHER
20 WELL-KNOWN CLOCK DISTRIBUTION SCHEMES.

21 IN THIS CASE ALSO, THE PATENT
22 SPECIFICATION DISCUSSES INVENTIONS USING A CLOCK
23 BEFORE THE PREFERRED CLOCK DISTRIBUTION SCHEME IS
24 ACTUALLY LAID OUT.

25 AND FIGURE 14, FOR EXAMPLE, IN THE

1 PATENT, WHICH WE MENTION IN OUR PAPERS, SHOWS A
2 CLOCK WHICH GOES TO A MASTER AND TWO DEVICES, IT
3 MUST BE A SYSTEM CLOCK, WHICH IS DISCUSSED BEFORE
4 THE PREFERRED CLOCK DISTRIBUTION SCHEME IS
5 DISCUSSED.

6 AND THEN --
7 COULD WE GO TO THE '263 PATENT. I DON'T
8 HAVE A PAGE NUMBER. I WANT TO GO TO COLUMN 18.
9 OH, HOLD ON. I CAN TELL YOU WHAT THAT IS. IT IS
10 PAGE 25.

11 AND -- OH, THAT'S WHERE WE WERE BEFORE.
12 IF WE COULD GO TO THE CLOCKING SECTION NEAR THE
13 BOTTOM OF THE RIGHT-HAND COLUMN.

14 SO AFTER DISCUSSING VARIOUS DISTINCT
15 INVENTIONS OPERATING WITH A CLOCK, THEN THE RAMBUS
16 SPECIFICATION TURNS TO THIS DISTINCT INVENTION.

17 "CLOCKING. CLOCKING A HIGH SPEED BUS
18 ACCURATELY WITHOUT INTRODUCING ERROR DUE TO
19 PROPAGATION DELAYS CAN BE IMPLEMENTED BY HAVING
20 EACH DEVICE MONITOR TWO BUS CLOCK SIGNALS AND THEN
21 DERIVE INTERNALLY A DEVICE CLOCK, THE TRUE SYSTEM
22 CLOCK."

23 I THINK HERE THE SPECIFICATION IS VERY
24 CLEAR THAT THIS IS A DISTINCT INVENTION THAT YOU
25 CAN USE IF YOU WEREN'T GOING TO USE THE PRIOR ART

1 CLOCK DISTRIBUTION SCHEMES WELL-KNOWN IN THE ART.

2 AND THE LAST POINT I WANT TO MAKE ABOUT
3 THAT IS THAT THIS WAS RECOGNIZED IN CONNECTION WITH
4 THE ORIGINAL RESTRICTION REQUIREMENT, THAT THIS WAS
5 A DISTINCT INVENTION BY, BY THE EXAMINER AT THE
6 PTO.

7 AND IF WE COULD PULL UP THE ORIGINAL
8 RESTRICTION REQUIREMENT, WHICH WAS ATTACHED TO
9 THIS, TO ONE OF MR. BROWN'S DECLARATIONS AS EXHIBIT
10 83.

11 THERE IT IS. AND LET'S GO TO PAGE 4.
12 AND COULD YOU BLOW UP STARTING AROUND THE MIDDLE.
13 ALL RIGHT. LET'S GO DOWN JUST A FEW MORE LINES.
14 STOP. LET'S GO UP A FEW MORE LINES, THEN WE'LL GO
15 DOWN.

16 ONE OF THE RESTRICTION REQUIREMENTS
17 IMPOSED HERE WAS BETWEEN GROUP I, WHICH INCLUDED
18 CLAIMS 1 TO 45 AND SOME OTHER CLAIMS IN THE PATENT,
19 AND GROUP III.

20 AND IN THE ORIGINAL RESTRICTION
21 REQUIREMENT, THE EXAMINER SAID, "GROUP I RELATES TO
22 A MEMORY AND BUS SUBSYSTEM, INCLUDING ADDRESS
23 REGISTER, TRANSCEIVERS, AND MEMORY SECTIONS, A, AND
24 GENERAL MENTION OF TIMING, BBR."

25 THEN IT GOES ON. "GROUP III IS THE

1 SUBCOMBINATION, PSP, WHICH IS A SPECIFIC CLOCKING
2 AND TIMING SCHEME."

3 AND IF YOU LOOK AT GROUP III, IT BEGINS
4 WITH CLAIM 73, AND IF YOU LOOK UP ORIGINAL CLAIM
5 73, YOU WILL SEE ESSENTIALLY THIS PREFERRED RAMBUS
6 CLOCK DISTRIBUTION SCHEME OF THE EARLY AND LATE
7 CLOCKS AND CALCULATING THE MID-POINT.

8 AND THEN THE EXAMINER GOES ON. "SINCE
9 CLAIMS TO BOTH THE COMBINATION AND SUBCOMBINATION
10 ARE PRESENTED AND ASSUMED TO BE PATENTABLE, THE
11 OMISSION OF THE DETAILS OF THE CLAIMED
12 SUBCOMBINATION IN THE COMBINATION ABBR, IS EVIDENCE
13 THAT THE PATENTABILITY OF THE COMBINATION DOES NOT
14 RELY ON THE DETAILS OF THE SPECIFIC
15 SUBCOMBINATION."

16 THIS IS AN EXPLICIT RECOGNITION BY THE
17 EXAMINER THAT YOU, THAT THE GROUP I CLAIMS, WHICH
18 HAD ONLY A GENERAL MENTION OF TIMING, DID NOT HAVE
19 TO USE THE PREFERRED CLOCK DISTRIBUTION SCHEME
20 WHICH WAS CLAIMED SEPARATELY AND WHICH WAS MADE
21 SUBJECT TO A RESTRICTION REQUIREMENT.

22 THE COURT: WHAT'S YOUR COMMENT, IF ANY,
23 WITH RESPECT TO THE SYNCHRONOUS MEMORY DEVICE
24 DEFINITION THAT I GAVE YOU TODAY?

25 MR. DETRE: WE WOULD LIKE THE

1 OPPORTUNITY, YOUR HONOR, TO SUBMIT A PAPER ON THAT
2 ON FRIDAY.

3 THE COURT: OKAY.

4 MR. DETRE: AND YOUR HONOR HAD MENTIONED
5 THAT --

6 THE COURT: YEAH. LET'S LET --
7 MR. BROWN, DID YOU HAVE ANYTHING ELSE BEFORE WE
8 BREAK?

9 MR. BROWN: YES, I DID, YOUR HONOR.

10 RAMBUS MISCONSTRUES OUR ARGUMENT ON THE
11 SYNCHRONOUS MEMORY, ON THIS SYNCHRONOUS MEMORY
12 DEVICE, AND WHETHER OR NOT THIS PARTICULAR CLOCKING
13 SCHEME IS SOMETHING THAT COULD BE SEPARATELY
14 PATENTABLE REALLY MISSES THE POINT ENTIRELY.

15 THE ONLY CLOCKING SCHEME WHICH IS
16 DISCLOSED IN THE PATENT IS THIS EARLY CLOCK, LATE
17 CLOCK SCHEME.

18 SO THAT THE ONLY -- THE ONLY -- THE ONLY
19 SCHEME, THE ONLY CLOCKING SCHEME IS ONE WHERE THERE
20 ARE TWO CLOCKS WITH DIFFERENT TIMING INFORMATION,
21 AND THERE ARE NO OPERATIONS OF THE INTERNAL, THE
22 INPUTS, THE OUTPUTS THAT TAKE PLACE WITH RESPECT TO
23 ONE OF THOSE EXTERNAL CLOCKS.

24 AND IN OUR INITIAL VIEW, WE THINK THAT
25 THE PROPOSED DEFINITION THAT YOU POSTED ON THE

1 BOARD IS FINE ON SYNCHRONOUS MEMORY DEVICE.

2 BUT IT ONLY RECITES ONE EXTERNAL CLOCK,
3 AND THE DEFINITION -- WE AGREE THAT IT'S AN
4 APPROPRIATE MARKMAN DEFINITION, BUT BASICALLY
5 THERE'S NO SUPPORT FOR IT IN THE RAMBUS DISCLOSURE
6 BECAUSE THERE'S NO EMBODIMENT OF ANY CLOCKING
7 SCHEME IN THE RAMBUS DISCLOSURE THAT HAD, THAT DOES
8 INPUTS AND OUTPUTS OR REFERENCES ANY OPERATIONS
9 WITH RESPECT TO JUST ONE EXTERNAL CLOCK.

10 THE COURT: OKAY.

11 MR. BROWN: OKAY. AND YOU MENTIONED THAT
12 THERE WERE SOME OTHER ISSUES THAT YOU WANTED
13 ADDITIONAL INFORMATION ON.

14 THE COURT: MOST OF IT HAS BEEN COVERED,
15 BUT I WOULD LIKE YOUR RESPECTIVE COMMENTS ON MY
16 REVISED PROPOSED SYNCHRONIZED MEMORY DEVICE; AND I
17 THINK IT WOULD BE HELPFUL IF YOU BOTH DEFINE FOR ME
18 A PACKET.

19 I THINK THAT'S IT.

20 MR. DETRE: YOUR HONOR, WOULD YOU LIKE
21 THOSE BOTH BY FRIDAY?

22 THE COURT: IF YOU COULD.

23 MR. BROWN: OKAY.

24 MR. DETRE: WE WILL.

25 THE COURT: OKAY.

1 MR. BROWN: THANK YOU, YOUR HONOR.

2 THE COURT: THANK YOU.

3 MR. DETRE: YOUR HONOR, EXCUSE ME. DO I
4 UNDERSTAND, THEN, THAT WE WON'T BE DOING ANYMORE
5 BRIEFING ON READ REQUEST?

6 THE COURT: UM --

7 MR. DETRE: IT'S OUR POSITION THAT IT'S
8 BEEN FULLY BRIEFED AND ARGUED AND NO FURTHER
9 BRIEFING IS REQUIRED.

10 THE COURT: YOU DIDN'T WANT TO DO MORE,
11 DID YOU? OR DID YOU?

12 MR. BROWN: NO. I JUST THOUGHT THAT IF
13 YOU -- I WAS OFFERING TO DO MORE IF YOU THOUGHT IT
14 WOULD BE OF ANY ASSISTANCE.

15 THE COURT: I THINK IT'S BEEN PRETTY WELL
16 HASHED OUT.

17 MR. BROWN: WELL, IT'S BEEN HASHED OUT AT
18 LENGTH, ANYWAY.

19 THE COURT: OKAY. THANK YOU.

20 MR. DETRE: THANK YOU, YOUR HONOR.

21 MR. BROWN: THANK YOU.

22 (WHEREUPON, THE PROCEEDINGS IN THIS
23 MATTER WERE CONCLUDED.)

24

25

