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ORIGINAL

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR U.K. LTD., and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH,

Plaintiffs,

vs.

RAMBUS INC.,

Defendant.

CASE NO. CV 00-20905 RMW

REPLY DECLARATION OF ROBERT J. MURPHY IN SUPPORT OF RAMBUS'S MOTION FOR SUMMARY JUDGMENT

Date: **March 23, 2004**
Time: **9:00 a.m.**
Ctrm: **6 (Hon. Ronald M. Whyte)**

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DECLARATION OF ROBERT J. MURPHY

I, ROBERT J. MURPHY, declare as follows:

1. I have been asked to review and offer my opinions as to the Declaration of David L. Taylor in Opposition to Rambus's Motion for Summary Judgment of Infringement (Taylor Decl.).

2. Two standard modes of reading DRAM have been in use since the early days of DRAM devices. In asynchronous DRAMs, a "normal" access involves providing a row address on the address pins, latching that address using the RAS\ strobe and providing that address information to the row decoders to select a particular row to access. That action is followed by providing a column address on the address pins, latching that address using the CAS\ strobe and providing that address information to the column decoders to select one or more particular columns to access. The row and column information selects a specific piece of data which is then sent to the output buffers for delivery outside the device. The process is then repeated in its entirety to obtain the next piece of data.

3. "Page mode" access is different. In page mode access, the DRAM uses the row address and RAS\ to select all of the pieces of data on that row (i.e. all columns) and hold them so as to be available to the user whether the user submits one column address (as in normal mode) or multiple column addresses in either sequential or random order. The row is thus viewed as a "page of data," and the user can request any piece of data on the page. The DRAM simply holds all of the pieces of data and with each new column address and CAS\ strobe delivers new data corresponding to the given column address. This can continue for a few column addresses or until the whole "page" is read as determined by the user. Synchronous DRAMs operate in a similar manner, but they base their operations on the operation codes delivered over the control lines and the associated addresses, sampled synchronously with the clock, rather than monitoring the states of asynchronous signals like RAS and CAS.

4. I disagree with Mr. Taylor's assertion that the set of signals sampled from the /CS, /RAS, /CAS, /WE, and A10 pins of the accused devices is not a "series of bits used to request a

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read of data" because these signals are "received at the same time" rather than over "several clock cycles." Taylor Decl. ¶ 23. In fact, in an embodiment described in the patent specification, the "read request" is itself a set of bits, identified as the "AccessType" field, transmitted in parallel and received during one clock cycle. '263 patent, Fig. 4.

5. According to Mr. Taylor, the packet-based interface used in the Rambus patents "receives bits in fields of a (request) packet which occupies several clock cycles." Taylor Decl. ¶ 23. Mr. Taylor's conclusion, that the bits corresponding to a "read request" are received over several clock cycles is incorrect because a "request packet" is not a "read request." In the embodiment illustrated in Figure 4 of the patent specification, a "read request" is a series of bits received in parallel within a request packet; the entire request packet contains other information besides the "read request" that is received in later clock cycles.

6. The words "series of bits" describes the group of bits (e.g., as shown in Figure 4 of the patent) directing the memory device to perform a specific "type" of read operation. In the embodiment shown in Figure 4, this group of bits is transmitted not in a series of clock cycles, but rather in parallel during a single clock cycle. Since the Federal Circuit's definition of "read request" must (at a minimum) include the preferred embodiment that the court itself references as an example that meets with its definition, the words "series of bits" must be read in such a fashion as to include a "group of bits transmitted in parallel" as is demonstrated in the embodiment shown in Figure 4.

7. In fact, the words "series of bits" does not suggest to a person of skill in the art that the bits must be received following one another in time. A series of bits could refer to a particular ordering of bits in time, but it could also refer to a particular ordering of bits relative to one another when they are received at the same time. In this case, the signals received on the /CS, /RAS, /CAS, /WE, and A10 pins of the accused devices are a series of bits of the latter type – they are ordered relative to one another in the sense that that a permutation of the signals would in general result in a different instruction to the device, as is clear from the truth tables in Hynix's data sheets.

8. Therefore, the "series of bits used to request a read of data from a memory device

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where the request identifies what type of read to perform" as specified by the Federal Circuit includes a "group of bits transmitted in parallel" to direct a type of read to perform. Mr. Taylor acknowledges that the accused devices receive such a "group of bits." Taylor Decl. ¶ 23. As will be shown below, the accused devices also use the "read request" to identify what "type" of read to perform.

9. Mr. Taylor repeatedly implies that a read or write command can be transmitted to the accused Hynix devices without the AP (A10) bit:

> "At least two clock cycles later, the Read (RD) command is sent to the memory with the column address; the RD command consists of the following logic levels on the control lines: CS\=Low, RAS\=High, CAS\=Low, WE\=High." Taylor Decl. ¶ 12.

> "At least two clock cycles later, the Write (WR) command is sent to the memory with the initial column address of the cell(s) to be written to. This command consists of the following combination of control signals CS\=Low, RAS\=High, CAS\=Low, WE\=Low at the rising edge of the clock; . . . ." Taylor Decl. ¶ 13.

> "As discussed above in paragraph 12, the accused devices receive a Read (RD) command by simultaneously sensing the following combination of control signals CS\=Low, RAS\=High, CAS\=Low, WE\=High at the rising edge of the clock. The bus interface used in the accused products is a 'parallel' interface." Taylor Decl. ¶ 23.

However, all read and write commands listed in the Hynix documentation for the SDRAM and the DDR SDRAM accused devices provide that the logical value of the AP (A10) bit must be set (either high or low, depending on the "type" of read or write) to specify such a command, as Mr. Taylor acknowledges elsewhere. Taylor Decl. ¶¶ 14, 22. At no time can the AP (A10) bit act on its own and create a separate command. It is always decoded with the appropriate logic levels on

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CS\, RAS\, CAS\ and WE\ to identify a particular "type" of read or write.

10. According to Mr. Taylor, the combination of /CS, /RAS, /CAS, /WE, and A10 do not specify the "type of read to perform." I disagree. "Type" has a very broad definition and a read command with autoprecharge would be well understood by one of skill in the art to be a "type" of read.

11. Mr. Taylor also states: "The reading of data from memory chip is the same regardless of whether the bank being accessed is subsequently precharged. The subsequent precharge of the bank being accessed does not alter or affect the manner in which data was previously read from the memory chip – as instructed by the Read (RD) command." Taylor Decl. ¶ 22. In my opinion, this description of the operation of the accused devices is inaccurate. The "type" of read or write is defined by the AP (A10) bit, either a read or write with autoprecharge or without auto precharge. AP is a necessary part of a read or write command.

12. Reads with and without autoprecharge are different "types" for two reasons. First, as with "series of bits" above, the preferred embodiment of a "read request" that the Federal Circuit considered in construing the term included reading with and without autoprecharge as different types of reads. The AccessType field in a request packet, which corresponds to a "read request" in that preferred embodiment, includes information that "determines whether the DRAM should precharge the sense amplifiers or should save the contents of the sense amps for a subsequent page mode access." '263 patent, col. 10:30-33.

13. Second, contrary to Mr. Taylor's assertion, whether a read is with or without autoprecharge does affect the way the device performs and reads the data. The performance of the device is affected because a read with autoprecharge does not require additional commands to precharge the sense amplifiers for subsequent reads. The reading of data is also affected due to changes in actions that are allowed or prohibited by a read with autoprecharge. For example, a read cannot be interrupted when the read is of an autoprecharge "type," that is when the AP(A10) bit is high at the time that the command is recognized. Declaration of David L. Taylor in Support of Hynix's Motions for Summary Judgment, Ex. 66 (SDRAM Device Operation) at 7, Ex. 69 (DDR SDRAM Device Operation) at 9. This is in contrast to a read without

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autoprecharge which can be interrupted. Additionally, an autoprecharge type of read allows the read/precharge sequence of events to overlap. *Id.* Since the devices are pipelined, as soon as the data moves from the memory array into the next pipeline stage, precharging can begin without having to wait for a separate precharge command. This, in essence, gives precharging a head start, allowing precharging to occur while the data is still moving through the pipeline stages to the output pins – there is no concern about trying to issue a separate "precharge" command to the device at a precise time to try to achieve the same effect. Eliminating the need for a separate "precharge" command also frees up bandwidth on the control lines such that other requests to other banks or devices can occur, thus increasing overall system efficiency. In my opinion, the accused devices do receive "a series of bits used to request a read of data from a memory device where the request identifies what type of read to perform."

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct and that this declaration was executed on March 3rd, 2004 at Los Gatos, California.

Robert J. Murphy