United States District Court
For the Northern District of California

E-filed: 11/24/2008

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

RAMBUS INC., Plaintiff, v. HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION U.S.A., Defendants.	No. C-05-00334 RMW ORDER GRANTING IN PART AND DENYING IN PART RAMBUS'S MOTIONS FOR SUMMARY JUDGMENT OF INFRINGEMENT **[Re Docket Nos. 503, 505, 506, 507, 509, 510]**
RAMBUS INC., Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., Defendants.	No. C-05-02298 RMW **[Re Docket No. 355]**

United States District Court
For the Northern District of California

RAMBUS INC.,

Plaintiff,

v.

MICRON TECHNOLOGY, INC., and MICRON SEMICONDUCTOR PRODUCTS, INC.

Defendants.

No. C-06-00244 RMW

[Re Docket Nos. 200, 201]

Rambus has accused the Manufacturers[1] of infringing various patents. The court held a two-day claim construction hearing and issued an order interpreting the disputed claim terms. *Rambus Inc. v. Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946 (N.D. Cal. 2008). Pursuant to a case management order, Rambus also filed motions for summary judgment of infringement by the Manufacturers' various accused products. The Manufacturers oppose the motions.

Pursuant to another request from the court, Rambus has narrowed the number of claims at issue and the scope of accused products to be tried in January 2009. This order addresses only the motions and arguments directed at the claims and products subject to that trial.

The court has reviewed the papers and considered the arguments of counsel. For the following reasons, the court grants summary judgment as to direct infringement of claim 16 of the '295 patent (except as to Nanya's DDR3 SDRAM); denies summary judgment as to infringement of the other claims at issue; and grants summary adjudication in favor of Rambus in a number of the Manufacturers' non-infringement contentions.

I. BACKGROUND

A. The Accused DRAMs

The Manufacturers produce a variety of commodity DRAMs, ranging from the standard DDR2 and DDR3 SDRAMs to the graphics-specialized gDDR2, GDDR3, and GDDR4 SDRAMs to the proprietary Micron RLDRAM II. Rambus has largely agreed with the individual Manufacturers

[1] The court collectively refers to the Hynix, Micron, Nanya, and Samsung entities in this suit as "the Manufacturers."

with respect to the designation of representatives of each type of DRAM,[2] and the parties rely on the data sheets of the representative devices.

B. Reading a Datasheet's Timing Diagrams

The evidence supporting and opposing Rambus's motion for summary judgment primarily consists of the datasheets of the accused devices. The data sheets for each Manufacturers' device appear as exhibits to the Tolliver Declaration.[3] A datasheet describes a product in varying levels of detail. For example, the Manufacturers' product datasheets generally begin with an overview of the key features and parameters of the device. *See, e.g.*, Hyinx DDR2 at 4. A typical DRAM datasheet also includes a description of the different interface pins that send and receive signals to and from the outside world, typically a memory controller. *See, e.g., id.* at 8-9. The datasheet also discusses the DRAM's testing conditions, electrical properties, and physical profile or package, though these details are not relevant to this case. Some of the Manufacturers also provide supplements to the datasheets with additional detail on specific aspects of the DRAM. For example, Hynix publishes a

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[2] In general, the "agreements" are less than formal. They appear as exhibits to the declaration of Craig Tolliver. *See Rambus Inc. v. Hynix Semiconductor, Inc.*, C-05-00334 RMW, Docket No. 489 (N.D. Cal. Oct. 5, 2007). With Hynix, Rambus agreed that "Hynix part number HY5PS124(8,16)21 F will be representative, for purposes of the claims currently asserted against DDR2, graphics DDR2, and GDDR3 parts in Case No. C-05-00334, of all Hynix DDR2, graphics DDR2 (such as gDDR2), and GDDR3 parts, with the exception of the GDDR3 part with part number HYRS573225F." *Id.*, Ex. 27. Samsung's K4T1G084A product is representative of both Samsung's DDR2 and gDDR2 products. *Id.*, Ex. 29. Micron's representative parts are: MT44H8M32 U26W (GDDR3); MT47H16M16 U26A (DDR2); MT47H32M 16 U27A (DDR2); and MT49H32M9 F26A (RLDRAM II). *Id.*, Ex. 30. Nanya's representative DDR2 part is NT5TU64M8AE. *Id.*, Ex. 31.

Rambus does not appear to have stipulated to any representative DDR3 or GDDR4 parts with any Manufacturer. Instead, Rambus appears to have chosen data sheets it believes to be representative of each Manufacturers' products to support its motions for summary judgment with respect to those product generations. No Manufacturer objected that the data sheets chosen by Rambus fail to represent the DDR3 or GDDR4 generations of their products. Accordingly, the court accepts the DDR3 and GDDR4 data sheets submitted by Rambus as representative of the Manufacturers' corresponding product generations for the purposes of this motion.

Going forward, the parties must reach agreement on what parts will be tried to the jury in the January trial, the fewer the better. These stipulations must be contained in the parties' joint pretrial conference statement.

[3] The data sheets appear as Exhibits 1 to 26 to the Tolliver Declaration. For example, the data sheets for Hynix's representative DDR2 part are Exhibits 1 and 2. Throughout this order, the court cites to these datasheets as "[Manufacturer] [Generation]." For example, the court refers to Exhibit 1 as "Hynix DDR2." Exhibit 2, the operation guide to the Hynix DDR2 SDRAM, is referred to as "Hynix DDR2 Operation."

"DDR2 SDRAM Device Operation & Timing Diagram" that supplies substantially more detail about how its product operates. *See generally* Hynix DDR2 Operation.

A common feature in the datasheets is a series of timing diagrams, which are specialized graphs showing the state of various signals over a period of time. As much of the evidence related to infringement relies on interpreting timing diagrams, a brief explanation follows. The graph below depicts a burst read operation in a Hynix DDR2 SDRAM:

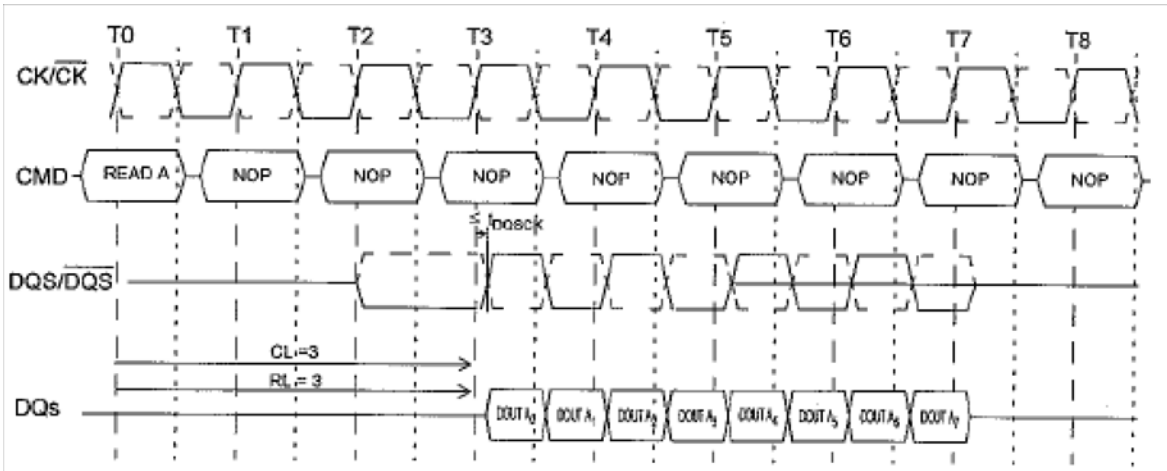

Figure 20. Burst read operation: RL =3 (AL=0, CL=3, BL=8)

The graph shows the activity of four types of signals. The top signal CK/CK\ illustrates the differential clock signal received by the DRAM. *See* Hynix DDR2 at 8. The second generally depicts the command received by the DRAM ("NOP" is shorthand for "no operation").[4] The third signal shown above is DQS/DQS\, the differential data strobe. Finally, the bottom graph ("DQs") represents the status of the multitude of data lines.[5]

Time progresses from left to right, marked by periods of the external clock signal. For

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[4] At a more granular level, the status of the "command" shown in the graph is determined by the status of four input pins: /RAS (row address strobe), /CAS (column address strobe), /WE (write enable) and /CS (chip select). The read operation shown in the diagram consists of a low voltage signal on /CAS and /CS with a high voltage signal on /RAS and /WE. *See* Hynix DDR2 Operation at 22.

[5] To clarify, "DQ" refers to an input/output pin for transmitting data. "DQs" is shorthand for referring to multiple data lines. It is critical to distinguish this from "DQS," the data strobe that plays a role in the input and output of data. "DQS" is not a data signal. It is a signal that provides timing information related to the data.

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example, "T1" marks the first complete period of the clock signal. The dashed line dividing each clock period into halves represents the crossing point of the clock signal and its complement (CK\). The ability to extract a timing signal from two points of a single clock period is what makes a DDR SDRAM "double data rate." *Accord* Murphy Decl. ¶¶ 86-89; *see, e.g.*, Hynix DDR2 at 4.

Finally, a timing diagram's captions often convey the state of multiple parameters that influence the DRAM's operation. In the figure above, "RL" means "read latency," which is the delay between the DRAM receiving instructions to begin a read operation and the DRAM making data available on the DQ pins to be read. A read latency of three implies that the DRAM waits three clock cycles before making data available to be read. In a DDR2 SDRAM, the read latency is equal to the sum of the programmable CAS latency ("CL") and the programmable additive latency ("AL," also referred to as "Posted CAS"). *See, e.g.*, Hynix DDR2 Operation at 19. In other words, RL = CL + AL. Finally, "BL" represents the "burst length" or duration of a given read or write operation. In the read operation shown above, the DRAM was programmed with a burst length of 8, hence 8 bits of data are made available in response to the read operation.

II. LEGAL STANDARD

Ninth Circuit law governing summary judgment procedures applies because this procedural law does not relate to substantive patent law principles. *In re Cygnus Telecomm'ns Tech., LLC, Patent Litig.*, 536 F.3d 1343, 1351-52 (Fed. Cir. 2008); *see, e.g., Exigent Tech., Inc. v. Atrana Solutions, Inc.*, 442 F.3d 1301, 1307-09 (Fed. Cir. 2006) (parsing regional circuit law of summary judgment). Rambus, as the party asserting infringement, bears the burden of persuasion at trial as to whether or not each of the Manufacturers' accused products infringe its claims. *L & W, Inc. v. Shertech, Inc.*, 471 F.3d 1311, 1317-18 (Fed. Cir. 2006). Thus, as the moving party, Rambus bears the burden of producing evidence showing that each device satisfies each limitation of each claim that the device is alleged to infringe. *Id.* at 1318. If Rambus fails to meet this burden of production, the Manufacturers need not produce anything to defeat summary judgment. *Nissan Fire & Marine Ins. Co., Ltd. v. Fritz Companies, Inc.*, 210 F.3d 1099, 1102-03 (9th Cir. 2000). If Rambus satisfies its burden of production, the Manufacturers must produce evidence such that a jury, drawing all

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inferences in favor of the Manufacturers, could find that the Manufacturers' accused products do not infringe the claim at issue. *Id*. If the Manufacturers produce such evidence, the motion must be denied. *Id.* A failure by the Manufacturers to adduce such evidence, however, entitles Rambus to summary judgment. *Id.*

Because Rambus bears the ultimate burden of persuasion on infringement at trial, the Manufacturers suggest that Rambus must not just produce evidence of infringement, but rather "an affirmative showing so compelling that no rational jury would fail to award judgment," i.e., evidence that is "conclusive" of infringement. *Synbiotics Corp. v. Heska Corp.*, 137 F. Supp. 2d 1198, 1201-02 (S.D. Cal. 2000). To an extent, the court agrees. It is Rambus's burden to present sufficient evidence such that a reasonable jury could not fail to find infringement. But the word "reasonable" is critical. A non-movant cannot avoid summary judgment by suggesting that a reasonable jury might not credit the movant's evidence. On this point, the court strongly disagrees with sources that argue that summary judgment is inappropriate in a patent case that involves "technical facts" or "expert testimony." *See, e.g.,* 10B Wright, Miller & Kane, Fed. Prac. & Proc. § 2732.1 (3d ed. 2008); *Vermont Structural Slate Co. v. Tatko Bros. Slate Co.*, 233 F.2d 9, 10 (2d Cir. 1956). Absent some indication in the movant's proffer that its expert testimony might be unreliable, *cf. Adickes v. S.H. Kress & Co.*, 398 U.S. 144 (1970), a reasonable jury would credit the only evidence it is given. Thus, an expert's credibility is material, and hence an issue for the jury, only if an opposing expert or other evidence actually contradicts the expert's testimony *as to a factual matter*.

This emphasis is important for two reasons. First, an expert's opinion must be supported by facts to support or defeat a motion for summary judgment. The Federal Circuit has held that an expert's "unsupported conclusion" as to whether there is infringement or whether a claim limitation is satisfied is not sufficient. *Arthur A. Collins, Inc. v. N. Telecom Ltd.*, 216 F.3d 1042, 1046-48 (Fed. Cir. 2000). Instead, the expert must "set forth the factual foundation for his opinion – such as a statement regarding the structure in the accused product – in sufficient detail for the court to determine whether that factual foundation would support a finding of infringement under the claim construction adopted by the court, with all reasonable inferences drawn in favor of the non-movant."

Id. at 1047-48; *see, e.g., Goldenberg v. Cytogen, Inc.*, 373 F.3d 1158, 1169 (Fed. Cir. 2004) (reversing grant of summary judgment and remanding for trial on non-literal infringement in light of expert testimony). This standard is important here because the parties largely rely on the declarations of their technical experts to support or oppose the instant motions.

Second, where two experts disagree about infringement, but do not dispute the facts regarding the accused device or method, the question of infringement is more appropriately viewed as a legal question of claim construction. *See MyMail, Ltd. v. America Online, Inc.*, 476 F.3d 1372, 1378 (Fed. Cir. 2007) ("Because there is no dispute regarding the operation of the accused systems, that issue reduces to a question of claim interpretation and is amenable to summary judgment."); *Rheox v. Entact, Inc.*, 276 F.3d 1319, 1324 (Fed. Cir. 2002); *General Mills, Inc. v. Hunt-Wesson, Inc.*, 103 F.3d 978, 983 (Fed. Cir.1997); *but see Int'l Rectifier Corp. v. IXYS Corp.*, 361 F.3d 1363, 1375 (Fed. Cir. 2004) (suggesting otherwise).[6] Here, the parties largely agree about the structure and function of the accused DRAMs, but dispute how the court's construction of Rambus's claims apply to those structures and functions. These disputes thus collapse into questions of law for the

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[6] The *International Rectifier* opinion appears to be an outlier. It distinguishes *General Mills* on the following basis: "In *General Mills*, however, the parties agreed with each other and the district court about how each of two competing claim constructions would apply to the undisputed structure of the accused invention." 361 F.3d at 1375. The *International Rectifier* court does not supply a pin cite for this statement about *General Mills*, and the *General Mills* opinion does not appear to mention any such agreement or stipulation. On the contrary, the appellant in *General Mills* "assert[ed] that the district court erred in granting summary judgment of literal noninfringement with respect to the structural limitations of claims 1 and 7 [and] argued that the district court improperly resolved genuine issues of material fact, did not consider claims 1 and 7 separately, and misconstrued various structural limitations of claims 1 and 7." 103 F.3d at 983. Had the parties stipulated to the outcome under the different proposed claim constructions, it would seem odd for the appellant to have raised the issue of the court improperly resolving questions of fact. Thus, the reasoning of *International Rectifier* is unclear.

Another court has noted the incongruity between these cases. *Rice v. Honeywell Int'l, Inc.*, 494 F. Supp. 2d 487, 489-90 (E.D. Tex. 2007). The *Rice* court suggested that while the parties in *International Rectifier* stipulated to the accused product's shape, the court still found the record too undeveloped to determine infringement as a matter of law. 494 F. Supp. 2d at 490. On the other hand, the *International Rectifier* court did remand with instructions to enter summary judgment of non-infringement as to one limitation. *Id.* at 490-91 (citing *Int'l Rectifier*, 103 F.3d at 1375). This reading of *International Rectifier* suggests that the Federal Circuit may not have intended to limit the otherwise well-entrenched rule that where there is no dispute regarding the operation of the accused device, the issue of literal infringement collapses into a question of claim construction amenable to summary judgment.

court to resolve.

III. INFRINGEMENT ANALYSIS

Rambus must establish *facts* that show that each accused product embodies each limitation of each claim the product is alleged to infringe. To meet its burden, Rambus relies on its technical expert Robert J. Murphy, an electrical engineer, to explain DRAM technology and interpret the data sheets and technical specifications of the accused DRAMs. The Manufacturers rely on their technical expert, Joseph McAlexander, also an electrical engineer, to rebut Rambus's showing.[7] Because Rambus must make a *prima facie* showing that the accused devices practice each limitation, the court's analysis begins with Rambus's proffer of evidence as to each claim. The following table summarizes the allegations and the court's holdings:

Asserted Patent No.	Claim	Summary judgment sought? Granted?	Accused Product Generations
6,182,184	14	Yes / No	DDR2, DDR3, gDDR2, GDDR3
6,266,285	16	Yes / Yes	DDR2, DDR3, gDDR2, GDDR3, GDDR4
6,314,051	27	Yes / No	DDR2, DDR3, gDDR2, GDDR3, GDDR4, RLDRAM II
6,314,051	43	Yes / No	DDR2, DDR3, gDDR2, GDDR3, GDDR4, RLDRAM II
6,324,120	33	Yes / No	DDR2*, DDR3, gDDR2*, GDDR3*
6,378,020	36	Yes / No	DDR2*, DDR3, gDDR2*, GDDR3*, GDDR4
6,426,916	28	Yes / No	DDR2*, DDR3, gDDR2*, GDDR3*
6,452,863	16	Yes / No	DDR2*, DDR3, gDDR2*, GDDR3*
6,546,446	3	Yes / No	DDR2, DDR3, gDDR2, GDDR3, GDDR4
6,546,446	4	No / NA	DDR2, DDR3, gDDR2, GDDR3, GDDR4
6,584,037	34	Yes / No	DDR2, DDR3, gDDR2, GDDR3, GDDR4
6,751,696	4	Yes / No	DDR2, DDR3, gDDR2, GDDR3, GDDR4, RLDRAM II
* These Hynix and Micron product generations are not accused of infringing these claims in this action.			

[7] The court refers to the following declarations throughout the order: *Rambus Inc. v. Hynix Semiconductor, Inc.*, C-05-00334, Docket No. 495 (N.D. Cal. Oct. 5, 2007) ("Murphy Decl."); Docket No. 662 (Nov. 2, 2007) ("McAlexander Decl."); Docket No. 726 (Nov. 16, 2007) ("Murphy Reply Decl.").

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A. Claim 16 of the '285 Patent

1. The Asserted Claim

Rambus asserts that the Manufacturers' accused products infringe claim 16 of U.S. Patent No. 6,266,285. Murphy Decl. ¶¶ 174-77; *see id.* ¶¶ 150-73. The claim *generally* recites a method of operating a memory device involving: (1) receiving an external clock signal, (2) receiving a delay time value and storing it in a register, (3) receiving a request for a write operation, and finally (4) sampling data in response to the write operation after the delay time transpires. Rambus colloquially refers to this claim as covering the implementation of programmable write latency. The full text of the claim follows, with the language of the claim from which it depends incorporated in brackets:

> [[A method of operation in a memory device having a section of memory which includes a plurality of memory cells, the method comprising:
>
> receiving an external clock signal;
>
> receiving a request for a write operation synchronously with respect to the external clock signal; and
>
> sampling data, in response to the request for a write operation, after a programmable number of clock cycles of the external clock signal transpire.]]
>
> [further including storing a value which is representative of the programmable number of clock cycles of the external clock in a programmable register on the memory device.]
>
> further including receiving a set register request, wherein in response to the set register request, the memory device stores the value in the register.

2. The Evidence With Respect to Each Limitation

In this section, the court determines whether Rambus has met its burden of production with respect to the Hynix DDR2 SDRAM. Rambus similarly supports its burden of production with respect to each other device accused of infringing this claim and with respect to each Manufacturer. The sole exception is Rambus's showing with respect to Nanya's DDR3 SDRAM, which is discussed in more detail *infra*.

a. A Memory Device With a Plurality of Memory Cells

Mr. Murphy states that Hynix's DDR2 SDRAM is a memory device with a plurality of memory cells. Murphy Decl. ¶ 150 (citing *id.* ¶¶ 45, 50). He supports this conclusion by reference

to Hynix's DDR2 data sheets. The Hynix DDR2 SDRAM comes in a variety of configurations, but all include four memory banks. Hynix DDR2 at 5-7. Each of these banks contains memory cells for storing information. Murphy Decl. ¶¶ 22, 23. As a 512 Mb device, the representative Hynix DDR2 SDRAM contains over 500 million memory cells, *see* Murphy Decl. ¶ 23; Hynix DDR2 at 4, and a number in excess of 500 million easily satisfies the "plurality" requirement. Rambus has therefore met its burden of producing facts establishing that the accused products embody this preambulary limitation. The Manufacturers do not argue that their devices do not satisfy this limitation.

b. Receiving an External Clock Signal

Mr. Murphy next states that Hynix's DDR2 device receives an external clock signal. Murphy Decl. ¶ 151. The data sheet confirms this. Each DDR2 configuration includes interface pins for CK and CK\. Hynix DDR2 at 5-6 (pins E8 and F8), 7 (pins J8 and K8). In its description of these pins, the data sheet explains that they are the "differential clock inputs." *Id.* at 8. The clock inputs determine when the DRAM samples address and control signals, and data sampling "is referenced" (more on this later) to the clock signals. *Id.* Dozens of timing diagrams in the data sheets include a graph showing the differential clock signals. These graphs confirm the clock signals' periodic nature and their role in providing timing information. *See, e.g.*, Hynix DDR2 at 23 (shown above). Rambus has plainly shown that the accused devices embody this limitation, and again, the Manufacturers do not dispute this given the court's construction of the phrase. *But see Rambus*, 569 F. Supp. 2d at 981-85 (disputing the construction of "external clock signal").

c. Receiving a Request for a Write Operation

Whether the accused devices receive a "request for a write operation" synchronously with respect to the external clock signal is a disputed legal matter, but there is no dispute as to the facts. A write cycle begins on a rising edge of the clock when the DRAM receives a high voltage signal on the /RAS pin and low voltage signals on /CS, /CAS, and /WE pins. Murphy Decl. ¶ 76; Hynix DDR2 Operation at 19. The data sheet defines these input pins as command signals. Hynix DDR2 at 8 (noting that "/CS is considered part of the command code" and that /RAS, /CAS, and /WE are "command inputs"). As such, they are sampled at the crossing point of the differential clock signals.

See id. ("All . . . command inputs are sampled on the crossing of the positive edge of CK and negative edge of CK\."). This direct connection establishes the "known timing relationship" between receiving the four command signals and the external clock signal that satisfies the "synchronously with respect to" requirement. The Manufacturers do not dispute that the combination of a high voltage signal on /RAS and low voltage signals on /CS, /CAS, and /WE initiates a write cycle in their DRAMs.

Instead, the Manufacturers advance three arguments requiring interpretation of the court's claim construction. The court construed the phrase "request for a write operation" to mean "a series of bits used to request a write of data to a memory device where the request identifies what type of write to perform." *Rambus*, 569 F. Supp. 2d at 974-77. The Manufacturers raise issues requiring further interpretation of the terms "request," "series of bits," and "identifies what type of write to perform."

i. Does a "Request" Include Commands?

The Manufacturers note (and there is no dispute from Rambus) that a high /RAS signal and low /CS, /CAS, and /WE signals *require* the DRAM to sample incoming data signals and write them to the DRAM's memory arrays. Because the DRAM must respond in this manner, the Manufacturers dub this quartet of signals a write operation *command*. On the other hand, the Manufacturers label the quartet a *request* for a write operation if the DRAM can ignore or reject the memory controller's initiation of a write cycle. According to the Manufacturers, this mandatory/permissive distinction means that claim 16 only reads on methods of operating a DRAM where the DRAM may reject a memory controller's attempt to write data to a DRAM.

The Manufacturers base this semantic distinction on one aspect of the Farmwald/Horowitz specification common to all of the claims in suit. The specification discusses implementing a "retry format" that enables a DRAM to respond to a request for a read or a write with an error message if the DRAM cannot perform the requested read or write operation. *See generally* U.S. Patent No. 6,426,916, col. 12, ll. 8-50. The Manufacturers argue that because the Farmwald/Horowitz preferred embodiment can reject a read or write request by sending an error message, the word "request" in the

claims would be understood by a person of ordinary skill in the art to exclude signals sent to a DRAM that cannot be rejected. Mr. McAlexander testifies in support of this argument, noting that the operations of a DDR2 SDRAM are "mandated, not 'requested' by the external controller." McAlexander Decl. ¶ 45.

The specification does not distinguish requests from commands,[8] nor do the claims, and no party has presented any prosecution history shedding light on this dispute. Without intrinsic evidence, the court turns to extrinsic sources to determine how a person of ordinary skill would understand the word "request." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317-19 (Fed. Cir. 2005) (en banc). In gauging the relevance of such evidence, the court bears in mind (1) when the extrinsic source was created, (2) whether the extrinsic source was written by or for the person of ordinary skill in the art, (3) whether the extrinsic might be tainted or shaped by the bias of the pending litigation, (4) the significance of the extrinsic source within the enormous field of potential extrinsic sources of evidence, and (5) the impact the evidence has on public notice of the claim's scope. *See id.* at 1318.

Prior art patents, whether cited by any patent-in-suit or not, can be a useful guide to a term's ordinary meaning. *Arthur A. Collins*, 216 F.3d at 1044-45. First, they were initially written for the person of ordinary skill in the art. Second, their date is easily determined and compared to that of the patent-in-suit. Third, they are (normally) unconnected to the litigation and therefore lack the bias that can shade expert testimony. Here, Rambus points to a number of Micron SDRAM patents. To the extent these sources might show bias from having been created by a party, that bias would be against Rambus's position.

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[8] The word "command" appears in the Farmwald/Horowitz specification once. *See* '916 Patent, col. 11, ll. 44-51. In that section, the inventors describe programming the BlockSize[0:3] field in the preferred embodiment request packet used in the Rambus packet-based bus architecture. *Id.* If the DRAM received a sequence of four zeroes for BlockSize[0:3], it would indicate a block size 0 bits in length, essentially signaling that no data transfer would occur. This is not useful, so the inventors proposed configuring the DRAM to recognize BlockSize[0:3] = [0000] as a "special command" to refresh the DRAM or to switch DRAM access modes. This discussion is not helpful in resolving the issue raised by the Manufacturers, i.e., determining whether a person of ordinary skill in the art would understand "requests" to be permissive and "commands" to be mandatory.

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The Blodgett specification of several Micron patents[9] generally discusses a memory system including a microprocessor and a DRAM that attempts to reduce access times by anticipating the microprocessor's requests. One embodiment comprises "a microprocessor, a burst access memory having addressable memory cells for providing data in response to a *read request* from the microprocessor, the *read request* including a start memory cell address, and address generation circuitry for generating a memory cell address and initiating a read operation in anticipation of a read request from the microprocessor." U.S. Patent No. 6,601,156, col. 2, ll. 13-20 (emphasis added). This system has two parts: a microprocessor that transmits read requests and a memory that receives read requests (and attempts to anticipate future read requests). Two aspects of this embodiment and the discussion in the specification are worthy of note. First, the DRAM receives a request and that request causes the DRAM to begin the operation (at least until the address generation circuitry uses the memory cell address to take over and predict the next read operation). Second, there is no suggestion in the Blodgett specification that a DRAM may ignore the microprocessor's "request."

Another Micron patent describes a memory controller that can control the sequence of requests transmitted by the microprocessor. U.S. Patent No. 7,149,857 (filed May 14, 2002). Generally speaking, only a single row in a given bank of a DRAM may be accessed at a time. *See id.*, col. 1, ll. 26-40. If no row is activated, a "page miss" occurs and the bank must be activated (which takes time). *Id.* If the wrong row is open, a "page conflict" occurs and the wrong row must be closed ("precharged") and the correct row opened (which also takes time). *Id.* The ideal result (a "page hit") occurs when the row desired for an operation is the row that is already open. *Id.* Prior art memory systems processed requests in the order they were received, leading to a high mix of page misses and page conflicts and the longer access times they caused. *Id.*, col. 1, ll. 40-49. The invention of this Micron patent is a memory controller that can prioritize requests to improve access

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[9] The Blodgett application, filed on July 3, 1996, has given rise to, among others, U.S. Patent Nos. 6,601,156 (Jul. 29, 2003), 6,981,126 (Dec. 27, 2005), 7,210,020 (Apr. 24, 2007). While Rambus and Micron had a cool relationship at that point in time, the specification predates this dispute (understood broadly) by at least three and a half years.

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times by increasing the ratio of page hits to page misses and conflicts.

Rambus pulls a single quote from the specification's discussion of the queue of executed requests contained in the memory controller. *See* Murphy Reply Decl. ¶ 33. The queue "manages the requested data read from the DRAM upon execution of the *read requests*, and returns the requested data . . ." '857 Patent, col. 5, ll. 35-39 (emphasis added). To Rambus, this statement indicates that the DRAM executed the read operations and that these operations are known as "read requests."

This supports Rambus's interpretation, but it is not the most probative discussion in the patent. Part of the memory controller's process for optimally sequencing requests involves a "command sequencer." *See id.*, col. 4, ll. 48-61. That discussion recognizes that, for example, a read request can contain two components: a "read" command and a "data control command." *Id.* The data control command indicates whether to activate or precharge a row, while the read or write command indicates what operation to perform. *Id.* The command sequencer can optimize memory access by separating the read or write commands from their associated data control commands, transmit the data control commands in parallel with other commands and ahead of their associated read or write commands, and therefore increase the ratio of "page hits." *Id.*, col. 4, l. 62 – col. 5, l. 3. To the extent that a person of ordinary skill would distinguish a "request" from a "command," this discussion shows that the distinction is not the mandatory/permissive distinction urged by the Manufacturers. On the contrary, it shows that to a person of ordinary skill, a "request" for an operation may include certain details about that operation, in addition to the necessary "command" to accomplish it.

A final Micron patent's background discussion illustrates that Rambus is correct about the person of ordinary skill's understanding of a "request." In that background, the patent generally describes the timing of reading and writing data in SDRAM and DDR* SDRAMs. U.S. Patent No. 7,054,222, col. 1, l. 13 – col. 3, l. 59 (filed Jul. 19, 2004). In discussing the time it takes for an operation to transpire in an SDRAM, the time line begins with a "read *request* [being] specified at time T0." *Id.*, col. 1, ll. 37-41 (emphasis added). Later in the specification, the patent discusses a

"write command" signal that one skilled in the art would recognize as "a function of the RAS, CAS, and W/E signals external to the device." *Id.*, col. 6, ll. 13-19. The patent does not explicitly draw any distinction between "requests" and "commands," instead appearing to use them interchangeably.

"Learned treatises" can also help to ascertain a term's ordinary meaning. *Phillips*, 415 F.3d at 1317. A recent treatise strengthens the interpretation of the term proposed by Rambus. Bruce Jacob, Spencer W. Ng, & David T. Wang, *Memory Systems: Cache, DRAM, Disk* (2008) (hereinafter "Jacob, *Memory Systems*"). Before going further, the court notes that the treatise's "target audience are those planning to build and/or optimize memory systems: i.e., computer-engineering and computer-science faculty and graduate students (and perhaps advanced undergraduates) and developers in the computer design, peripheral design, and embedded systems industries." *Id.* at xxxiii. Though the treatise postdates the Farmwald/Horowitz patent by 18 years, it is from the same field and the court has found no indication that the meaning of any of the terms at issue have shifted during the art's evolutionary progression. The treatise appears authoritative within its field based on the court's failure to locate any treatises of a similar nature. Finally, the treatise does not appear to have been shaped by the pending litigation.[10] With these factors shaping the weight that can be placed on the text, the court turns to the book's discussions of "requests" and "commands."

The treatise's use of the phrase "request" at multiple points in the book reinforces Rambus's proposed construction and undermine the Manufacturers' proffered distinction. In an overview of DRAM organization, the authors discuss how a multi-bank design functions. *Id.* at 414-15. They note that the banks must share the same input and output pins, but that "the multibank architecture allows *commands such as read requests* to be pipelined." *Id.* at 414 (emphasis added). In a chapter on "Basic DRAM Memory Access Protocol," the authors discuss the interaction between different commands beginning with the "modern" DRAM (SDRAM). *See id.* at 437. Throughout the chapter,

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[10] Rambus suggests, but does not prove, that one of the authors consults for Nanya in this litigation. *See* Murphy Reply Decl. ¶ 33. Mr. Jacob has not previously appeared in this court. Nonetheless, any such affiliation would only suggest that the treatise's usage of words would be shaded in the Manufacturers' favor.

the authors appear to use the phrases interchangeably. For example:

> The case of consecutive read *commands* to different rows of the same bank has been examined in the previous section. This section examines the case of consecutive read *requests* to different banks with the second *request* hitting a bank conflict against an active row in that bank.

Id. at 440 (emphasis added).

If the treatise makes any distinction between a "request" and a "command," it is the distinction suggested in the Micron patent to request sequencing. The book's introductory definition of a memory controller's function is "to accept read and write requests to a given address in memory, translate the request to *one or more* commands to the memory system, [and] issue those commands to the DRAM devices in the proper sequence and proper timing[.]" *Id.* at 409 (emphasis added). In discussing basic command interactions, i.e., "without command reordering," the authors write "all of the DRAM commands associated with the first request must be scheduled before any DRAM commands associated with the second request can be scheduled." *Id.* at 440. With command reordering, the DRAM controller can take a read request, separate the read command from its associated precharge command, and "obtain better bandwidth utilization." *Id.* at 441. If there is any difference between the meaning of "request" and "command," these portions of the treatise suggest that it is that a request is composed of one or more commands; for example, a read request would contain a read command and may (or may not) contain other commands related to the status of the memory banks.

In the end, it appears that a person of ordinary skill would have used the terms "request" and "command" interchangeably. It is possible that a person of ordinary skill might have perceived a minor distinction between the terms, for example, that a read "request" would include a read "command" and the other necessary commands (like a precharge or bank activation command) to prepare the DRAM to carry out the read command. But nothing in the intrinsic evidence, the Micron patents, the Jacob treatise, or any other extrinsic source the court has encountered supports the Manufacturers' and Mr. McAlexander's mandatory/permissive distinction between "commands" and "requests."

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Based on the foregoing, a person of ordinary skill in the art would not understand the term "request" in "request for a write operation" to cover only instructions to the DRAM that the DRAM could reject. A person of ordinary skill would instead draw upon the common usage of the time, and still common in the art today, that a "request" is an instruction to a DRAM to perform an operation. There being no dispute that the quartet of signals discussed above initiates a write cycle in the Manufacturers' devices, the court concludes that Rambus has carried its burden of persuasion that the devices embody this aspect of the "request for a write operation" limitation.

ii. Does a "Series of Bits" Include High or Low Voltage States?

The court's construction of the "request for a write operation" limitation requires the DRAM to receive a "series of bits" that request a write of data. The Manufacturers argue that the four command inputs that begin a write cycle – a high voltage signal on /RAS and low voltage signals on /CS, /CAS, and /WE – do not constitute a "series of bits." The Manufacturers' entire argument on this point rests on the declaration of Mr. McAlexander. *See* Opp'n at 7-8. In Mr. McAlexander's opinion, the high or low voltage signals represent "states" of the signal lines and that a person of ordinary skill in the art would not consider these "states" to be "bits." McAlexander Decl. ¶ 61. Mr. McAlexander's sole reference to support his distinction is that the data sheets refer to the voltage levels as "states" in truth tables. *Id.* (citing Hynix DDR2 Operation at 50).

Mr. McAlexander's opinion that a high or low voltage state would not be understood by one of skill in the art as a "bit" is based on little more than his say-so. This substantially reduces its persuasive force, keeping in mind that such testimony is "generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence." *See Phillips*, 415 F.3d at 1317. Absent a basis rooted in intrinsic sources or extrinsic sources untouched by the litigation, an expert's naked opinion on the meaning of a term is of little help.

There is no support for Mr. McAlexander's opinion. Both general and technical dictionaries from around 1990 demonstrate that a high or low voltage state is a "bit." For example, a "bit" is a "contraction of the term 'binary digit'; a unit of information represented by a zero or a one." *IEEE*

Standard Dictionary of Electronic and Electrical Terms (4th ed. 1988); *The New IEEE Standard Dictionary of Electronic and Electrical Terms* (1993). It is "a unit of information equivalent to the result of a choice between two equally probable alternatives." *Webster's Third New International Dictionary* (1981). Or, in other words, it is "a unit of information derived from a choice between two equally probable alternatives or 'events.'" *Oxford English Dictionary* (2d ed. 1989). A final definition: "Bit is a contraction of the term Binary digIT. It is the smallest unit of information (data) a computer can process, *representing either high or low*, yes or no, or 1 or 0." *Newton's Telecom Dictionary* (4th ed. 1991) (emphasis added).

Even Mr. McAlexander's reliance on the Hynix' data sheet's truth table is misplaced. The truth table contains three entries: H (high), L (low), and X. *See* Hynix DDR2 Operation at 50. The data sheet defines X as "H or L (but a defined logic level)." *Id.*, n.6. Thus, although the truth table does not refer to the high and low voltage states on the command lines as "bits," it recognizes that "H" and "L" are defined as binary logic states. Because the data sheet defines the high and low states as logic levels, those "states" represent bits of information.

Finally, there is Mr. McAlexander's prior testimony. In an expert report from the *Infineon* litigation, Mr. McAlexander wrote that "[b]its are transmitted on signal lines by the use of voltage. A high voltage represents a '1' and a low voltage represents a '0'. Thus, examining the state of signal lines at a particular point in time is examining a series of bits . . . ." Murphy Reply Decl. ¶ 7.[11] In preparing the current declaration, Mr. McAlexander stated that he based his current opinion on the materials listed in Exhibit 1 to his October 5, 2007 declaration. *See* McAlexander Decl. § 5 (unnumbered paragraph). In the October 5, 2007 declaration, his first listed reference is "my prior reports identified in Exhibit 5." In Exhibit 5, he listed the eleven reports he filed in the *Infineon* litigation. Thus, the prior report quoted by Mr. Murphy served as a part of the materials Mr. McAlexander reviewed in preparing his current opinion, yet Mr. McAlexander makes no effort now

[11] Mr. Murphy did not include a copy of the report as an exhibit to his reply declaration. Nonetheless, the Manufacturers have not indicated that this statement is inaccurate in their supplemental briefing.

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to distinguish or explain his prior testimony that the voltage level of a command line represents a "bit."

In light of the foregoing, the argument advanced by the Manufacturers borders is without merit, and Mr. McAlexander's opinion is not credible. A person of ordinary skill in the art would recognize that the high voltage signal on /RAS and low voltage signals on /CS, /CAS, and /WE constitute a "series of bits."

iii. Are There Different "Types" of Write Requests?

Under the court's claim construction, the method of claim 16 requires the series of bits received by the DRAM to "identif[y] what type of write to perform." *Rambus*, 569 F. Supp. 2d at 974-77; *see also Rambus Inc. v. Infineon Techs., AG*, 318 F.3d 1081, 1093 (Fed. Cir. 2003) (construing "request"). The Manufacturers argue that their devices do not infringe the method because their devices only recognize one "type" of write operation. Implicit in the Manufacturers' argument is the notion that identifying what "type" of write requires there to be more than one. Rambus argues that the Manufacturers' devices meet this limitation because they feature two "types" of write operation: a write operation with auto-precharge and one without.

As discussed previously, a bank can only have one row open at a time. Before a new row can be opened, the old row must be closed, i.e., the bank must be "precharged." Hynix DDR2 Operation at 31, 36. The Hynix DDR2 SDRAM can be instructed to precharge a specific bank (or all banks) upon receiving a precharge command. *Id.* at 31. The combination of command signals that triggers a precharge operation is /CS, /RAS, and /WE low and /CAS high on a rising clock edge. *Id.* The status of address lines A10, BA2, BA1, and BA0 then determine which banks get precharged. *Id.* It is important to note that a precharge command and, for example, a write request, cannot be transmitted simultaneously because they require different statuses on the /CS, /RAS, /CAS, and /WE command lines. Thus, normal operation requires a precharge command to be sent on a first rising edge of the clock and then a write command to be sent on a second rising edge of the clock.

The Hynix DDR2 SDRAM includes the ability to recognize an "auto-precharge" command.

Id. at 36. When the DRAM receives a write command on the /CS, /RAS, /CAS, and /WE pins, it also monitors address input line A10. *Id.* "If A10 is LOW when the READ or WRITE command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence." *Id.* In other words, if A10 is low, auto-precharge is off, and following the operation, the bank does not automatically close. If the next request seeks to read or write to a different row in the same bank, a separate precharge command will be required before the next request can be processed. However, if the next request seeks to use the same row, that row will still be open. On the other hand, if A10 is high, the auto-precharge command accompanies the read or write operation. *Id.* Thus, once the write operation is complete, the DRAM will close the row, allowing it to proceed with a second request for a different row immediately. *See id.*

When construing the "request" terms at issue, the Federal Circuit held that the "request" must indicate its "type," listing as examples "page mode, normal mode, etc." *Infineon*, 318 F.3d at 1093. The Farmwald/Horowitz specification explains the distinction:

> The method of this invention provides for access mode control specifically for the DRAMs. One such access mode determines whether the access is page mode or normal RAS access. In normal mode (in conventional DRAMs and in this invention), the DRAM column sense amps or latches have been precharged to a value intermediate between logical 0 and 1. This precharging allows access to a row in the RAM to begin as soon as the access request for either inputs (writes) or outputs (reads) is received and allows the column sense amps to sense data quickly. In page mode (both conventional and in this invention), the DRAM holds the data in the column sense amps or latches from the previous read or write operation. If a subsequent request to access data is directed to the same row, the DRAM does not need to wait for the data to be sensed (it has been sensed already) and access time for this data is much shorter than the normal access time. Page mode generally allows much faster access to data but to a smaller block of data (equal to the number of sense amps). However, if the requested data is not in the selected row, the access time is longer than the normal access time, since the request must wait for the RAM to precharge before the normal mode access can start.

'916 Patent, col. 10, ll. 22-43. In other words, the claim is not directed to metaphysically different "types" of write operations. As construed by the Federal Circuit, the claimed "request for a write operation" always writes data the same way. The "types" of write operation differ in how they leave the memory bank with respect to the next request.

In light of that clarification regarding the meaning of "type," it is clear that the Hynix DDR2

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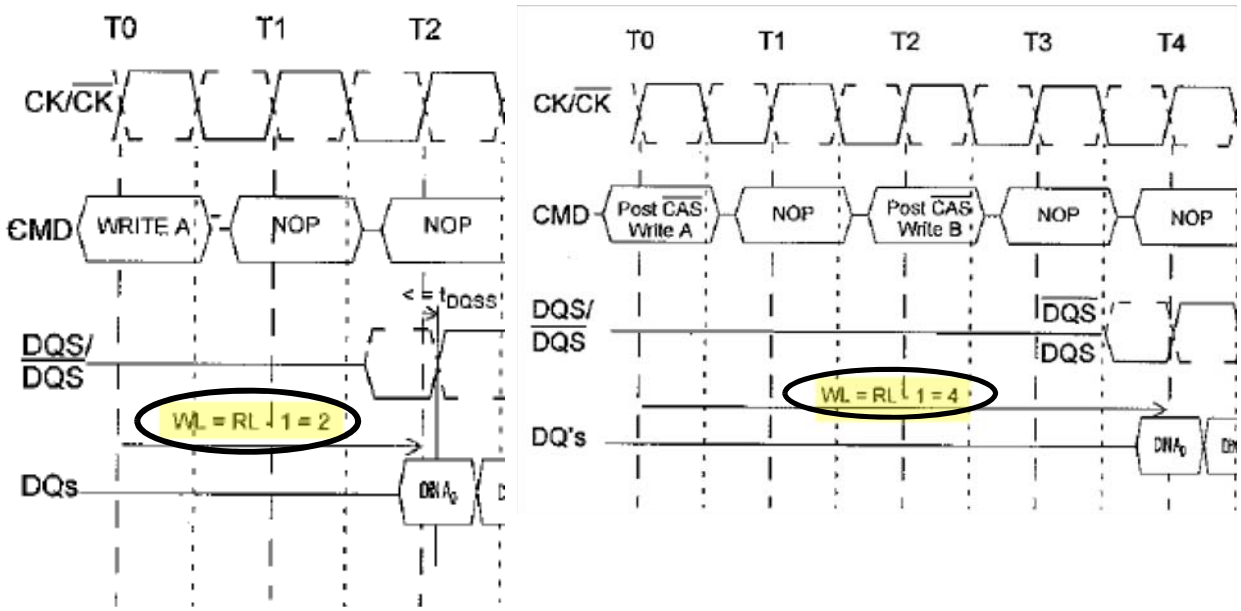
SDRAM (and other accused devices) embody this aspect of the limitation. A write operation with auto-precharge (i.e., with A10 high) closes the row following the write operation and enables the DRAM to operate analogous to the "normal" mode described in the specification and begin sensing data immediately after receiving the next request. A write operation without auto-precharge (A10 low) leaves the row open, risking a potential page conflict but permitting the faster page mode access described in the specification. Because the high or low signal sent over the A10 address input line specifies the "type" of write operation to perform, Rambus has carried its burden of persuasion with respect to this limitation.

d. Sampling Data After a Number of Clock Cycles

The next limitation of the claimed method requires the DRAM to sample data in response to the request for a write operation "after a programmable number of clock cycles of the external clock signal transpire." Mr. Murphy states that Hynix's DDR2 SDRAMs meet this limitation. Murphy Decl. ¶ 153.

He bases this opinion on his study of the Hynix DDR2's data sheet's discussion of the device's programmable write latency. *See id.* ¶ 71. As discussed above, the device has a write latency equal to the programmable read latency minus one clock cycle. Hynix DDR2 Operation at 20. The timing diagram examples in the data sheet illustrate what occurs in a write operation. *See id.* To begin, the DRAM receives a request for a write operation. It then waits for a number of clock cycles equal to the programmable write latency. Right before the latency period expires, the DQ strobe signal associated with data transfer becomes active. Finally, as the latency period expires, the DRAM begins to sample the DQ lines for incoming data. The two examples below show this process with write latencies of 2 and 4 clock cycles respectively:



Hynix DDR2 Operation at 26, 27 (emphasis added).

The Manufacturers dispute that this limitation is met because the DRAM samples data in response to the incoming DQ strobe. *See* McAlexander Decl. ¶ 143. As discussed in further detail below, the relationship between the external clock signal and the DQ strobe is not perfectly clear. As shown in Micron's Figure 29, the crossing point of DQ strobe jiggles about the crossing point of the complementary clock signals by what appears to be +/- t_{DQSS}. Thus, Mr. McAlexander appears correct that in some instances the DRAM might begin sampling data slightly before the write latency's number of clock cycles transpire.[12]

While this is true, it is irrelevant in light of the language of claim 16. The limitation reads: "sampling data, in response to the request for a write operation, after a programmable number of clock cycles of the external clock signal transpire." While such sampling may occur (slightly) before the write latency period transpires, at other times it will occur after the latency period transpires. This normal operation is shown in both examples above. The DRAM samples the data on the DQ lines at the crossing points of the DQ strobes, which occur after the latency period

[12] For context, the sampling never precedes the latency period number of clock cycles by more than a fraction of a single clock cycle.

transpires. The limitation is therefore met. That the accused devices occasionally fail to meet this limitation does not defeat the devices' infringement at other times. *See Hilgraeve Corp. v. Symantec Corp.*, 265 F.3d 1336, 1343 (Fed. Cir. 2001).

e. Storing the Programmable Value

A further limitation on claim 14 requires the DRAM to store a value "which is representative of the programmable number of clock cycles of the external clock in a programmable register on the memory device." Mr. Murphy states that the accused devices satisfy this limitation too, pointing to the programmable write latency value. Murphy Decl. ¶ 170.

The Hynix DDR2 SDRAM contains a programmable mode register that is configured when the DRAM is turned on. Hynix DDR2 Operation at 6. It is programmed by driving the command inputs /CS, /RAS, /CAS, and /WE and address inputs BA0 and BA1 to their low voltage state. *Id.* The CAS latency can then be set to 2, 3, 4, 5 or 6 clock cycles by varying the voltage levels on address inputs A4-A6. *Id.* In the extended mode register programming mode, the additive latency can be programmed from 0 to 5 clock cycles by controlling the voltage levels on address inputs A3-A5. *Id.* at 8. These values are stored in the mode register until the device is turned off, or until it is reprogrammed. *Id.* at 6.

As discussed, the read latency in the Hynix DDR2 SDRAM equals the CAS latency plus the additive latency. The write latency equals the read latency minus one clock cycle. The register therefore stores two values, which in turn represent the value of the write latency period. Rambus has therefore met its burden of producing facts establishing that the accused products embody this limitation. The Manufacturers do not argue that their devices do not satisfy this limitation.

f. Setting the Programmable Value With a Set Register Request

Finally, to practice the method of claim 14, the DRAM must also receive "a set register request, wherein in response to the set register request, the memory device stores the value in the register." The mandatory mode register and extended mode register programming discussed above embodies this limitation. *See* Murphy Decl. ¶ 174.

3. Lack of Evidence of Indirect Infringement

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Claim 16 of the '285 patent recites a method of operating a DRAM. Claim14 of the '184 patent, claim 16 of the '863 patent and claim 34 of the '037 patent are also method claims. The Manufacturers assert that Rambus has failed to address how the Manufacturers infringe those claims. As the Manufacturers point out, liability for indirect infringement is dependent upon the existence of direct infringement. *Joy Techs., Inc. v. Flakt, Inc.*, 6 F.3d 1306, 1308 (Fed. Cir. 1993). The mere act of selling or manufacturing a device that can practice the method but is capable of substantial non-infringing uses is not an act of infringement. *ACCO Brands, Inc. v. ABA Locks Mfrs. Co., Ltd.*, 501 F.3d 1307, 1313 (Fed. Cir. 2007). The Manufacturers thus argue that Rambus has provided no evidence that the Manufacturers have induced or contributed to any practice of the method of claim 16 of the '285 patent or any other of the method claims. Therefore, they argue that summary judgment must be denied.

Evidence of direct infringement is a technical hurdle to establishing indirect infringement of a method claim, but it does not appear that Rambus is claiming indirect infringement in its summary judgment motion. "In order to prove direct infringement, a patentee must either point to specific instances of direct infringement *or show that the accused device necessarily infringes the patent in suit*." *ACCO Brands*, 501 F.3d at 1313 (emphasis added). This latter path to establishing direct infringement is satisfied here. The evidence discussed at length above establishes that whenever a DDR2 SDRAM is turned on, it must have its mode register programmed. That mode register stores two values that together represent the programmable write latency. If the DRAM then receives data, i.e., has data written to it, it must receive a request for a write operation and sample the data following the write latency period. Throughout, it will have received a clock signal. Any operation of the Manufacturers' products necessarily infringes claim 16. The court assumes that the Manufacturers do not seriously contend that their products have not been used by themselves, as well as others. *See, e.g.*, Decl. of Sven Raz, *Rambus Inc. v. Hynix Semiconductor, Inc.*, C-05-00334, Docket No. 2425-10, Ex. 7 ¶¶ 49-60 (Expert Report of Robert Murphy). The court therefore enters partial summary judgment that claim 16 of the '285 patent is infringed by the Manufacturers' own use of their accused products.

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4. The Nanya DDR3 SDRAM Problem

As discussed before, Rambus has made the requisite showing of infringement of claim 16 with respect to each Manufacturers' accused device but one: Nanya's DDR3 SDRAM. This occurred because Rambus did not yet possess a Nanya DDR3 data sheet when it moved for summary judgment. Mr. Murphy nonetheless opines that Nanya's DDR3 device infringes the claim at issue because it is his understanding from an Intel website that Intel has validated Nanya's DDR3 parts. Murphy Decl. ¶ 30. Mr. Murphy reasons that Nanya's DDR3 "very likely includes the same features as the DDR3 SDRAMs of Hynix, Micron, and Samsung" for which Rambus has established infringement. Murphy Decl. ¶ 30. Given that the DDR3 devices must comply with the industry DDR3 standard, this is a reasonable inference. Yet the law is clear that Rambus "must make a *prima facie* showing of infringement as to each accused device before the burden shifts to the accused infringer to offer contrary evidence." *L & W*, 471 F.3d at 1318. As discussed above, the parties have sensibly stipulated that certain parts are representative of the many "flavors" of the types of DRAM that each Manufacturer produces. But no such stipulation exists between Rambus and Nanya regarding Nanya's DDR3 products. *See* Tolliver Decl., Ex. 31 (stipulating to a representative Nanya DDR2 product). Nanya has not agreed that its DDR3 products are identical to Hynix, Micron, or Samsung's, and without such an agreement, it is Rambus's burden to produce evidence establishing that. On this point, Mr. Murphy's belief that it is "very likely" that Nanya's devices are similar to Hynix, Micron, and Samsung's makes sense, but that belief is not enough to establish a *prima facie* case of infringement. Though Mr. Murphy provides more of a basis for his belief than the assumption discussed in *L & W*, it is not sufficient to meet Rambus's burden to produce evidence showing that Nanya's DDR3 products embody each limitation of the claims they are accused of infringing. Accordingly, the court denies Rambus's motion for summary judgment with respect to Nanya's DDR3 SDRAM. Nonetheless, the court anticipates that Nanya and Rambus can reach a stipulation with respect to Nanya's DDR3 SDRAMs to prevent unnecessary issues from having to be tried to the jury.

B. Claim 4 of the '696 Patent and Claim 3 of the '446 Patent

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Two of Rambus's asserted claims contain a limitation drawn to the output of data. For the reasons discussed below, Rambus has failed to carry its burden of production on infringement with respect to that limitation. The court therefore denies Rambus's motion for summary judgment with respect to claim 4 of U.S. Patent No. 6,751,696 and claim 3 of U.S Patent No. 6,546,446.

1. The Asserted Claims Covering Data Output

The two claims recite DRAMs that include output driver circuitry that output a first portion of data "synchronously with respect to a rising edge transition of the external clock signal" then output a second portion of the data "synchronously with respect to a falling edge transition of the external clock signal." *See* U.S. Patent Nos. 6,751,696 (claim 4); 6,546,446 (claim 3). In its claim construction order, the court adopted Rambus's proposed construction that "synchronously with respect to" means "having a known timing relationship with respect to." *Rambus Inc. v. Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946, 986-87 (N.D. Cal. 2008). Thus, to establish infringement of these two claims, Rambus must produce evidence that the accused DRAMs' output of data has a "known timing relationship" with respect to the rising and falling edge transitions of the external clock signal.

2. Rambus's Proffer of Evidence Regarding Data Output Timing

Mr. Murphy states that the Manufacturers' products "output data in response to (and synchronously with respect to) both the rising and falling edge transitions of an external clock signal." Murphy Decl. ¶¶ 86-89. To support his opinion, Mr. Murphy cites to the Manufacturers' various data sheets for their accused products.

a. Hynix

Mr. Murphy relies on the following timing diagram of a burst read command from the Hynix DDR2 operation guide:

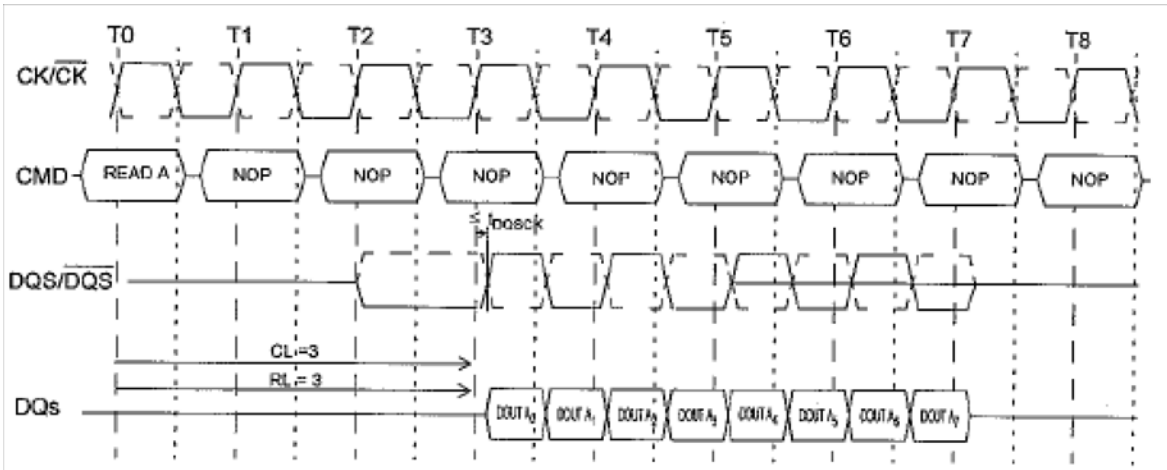


Figure 20. Burst read operation: RL =3 (AL=0, CL=3, BL=8)

Hynix DDR2 Operation at 22. Mr. Murphy's declaration does not explain the significance of the timing diagram; he merely cites it as support for his conclusion that the Hynix DDR2 SDRAM outputs data in response to the transitions of the external clock signal. What is clear from the face of the diagram is that the DRAM outputs data (represented by high or low voltage levels on the DQ pins) shortly after crossing points in the differential clock signals. What is not clear from the diagram is whether there is a "known timing relationship" between the transitions of the differential clock signals and the output of data.

Mr. Murphy cites two bullet points from the Hynix DDR2 datasheet's "key features" list to explain his conclusion. The first bullet point advertizes that "[o]n chip DLL align DQ, DQS and DQS\ transition with CK transition." Hynix DDR2 at 4. The second states that "[d]ata outputs on DQS, DQS\ edges when read (edged DQ)." *Id.* Mr. Murphy does not cite the bullet point reciting that "[a]ll addresses and control inputs except data, data strobes, and data masks latched on the rising edges of the clock." *Compare* Murphy Decl. ¶ 86 *with* Hynix DDR2 at 4. Mr. Murphy does not explain this language.

What is missing from Rambus's proffer is any evidence of the "known timing relationship" between the output of data and the external clock signal. Mr. Murphy's declaration does not explain the nature of the timing relationship between the external clock signal and outputting data from the

DRAM. His conclusion that the DRAM outputs data "synchronously with respect to" the transitions of the external clock signal must be factually supported. *Arthur A. Collins, Inc.*, 216 F.3d at 1047-48. With respect to Hynix's DDR2 SDRAM, that factual support consists of the diagram and the two bullet points from the key features list. But interpreting that factual foundation in a light favorable to the Manufacturers, as required in the summary judgment context, there is a triable issue as to whether there is a "known timing relationship" between the output of data and the external clock signal's transitions. To begin, the diagram hints at a connection between data output and the external clock signal, but data output correlates most strongly with transitions in DQ strobe, not the external clock signal. The data sheet list of "key features" cited by Mr. Murphy confirms this – the DRAM outputs data on the edges of DQS and DQS\, not CK and CK\. Hynix DDR2 at 4. Data output signals, unlike address and control signals, are not latched to the rising edges of the external clock signal. *Id.* Accordingly, Rambus has not met its burden of production because the scant evidence its relies upon could permit a jury to conclude that there is no "known timing relationship" between data output and the transitions of the external clock signal with respect to Hynix's products.

That is not say that the court embraces Mr. McAlexander's opposing conclusion that "data is not output from the memory as a result of the external clock signal." McAlexander Decl. ¶ 102. As noted in the key features list, the DRAM's delay lock loop circuitry aligns the transitions of the DQ strobe with the external clock signal. Hynix DDR2 at 4. Indeed, the timing diagram shown above marks the gap between the differential clock signals' crossing point and the DQ strobes' crossing point and indicates that it must be less than t_{DQSCK}. The list of timing parameters in the datasheet further indicates that this gap must not exceed +/- 400 picoseconds. Hynix DDR2 at 22. This suggests *some* timing relationship between the external clock signal and DQ strobe, though it cannot be determined on summary judgment whether there is a "known" relationship between them. *See* McAlexander Decl. ¶ 104.

The need for further testimony on this point is confirmed by Mr. Murphy's reply declaration, in which he purports to stand by his prior opinion, Murphy Reply Decl. ¶ 19, but appears to concede that data output occurs as a result of transitions in DQ strobe, Murphy Reply Decl. ¶ 21.

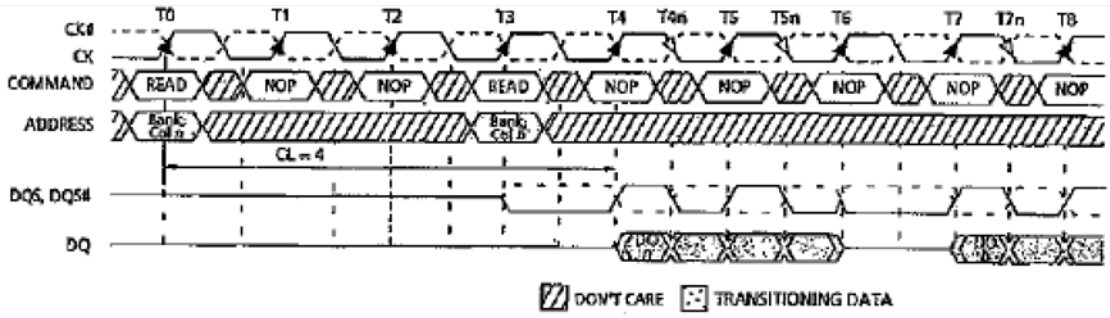
Nonetheless, Mr. Murphy concludes that because DQ strobe has a known relationship with respect to the external clock signal, the Manufacturers' products infringe by "simple transitivity." *Id.* ¶ 21. Mr. Murphy's reply declaration still fails to lay out adequately the nature of the "known timing relationship" between DQ strobe and the external clock signal to allow the court to understand it.[13] This will have to be done at trial.

b. Micron

Mr. Murphy's testimony regarding Micron's products is similarly conclusory. In its entirety, Mr. Murphy's testimony is that "[t]he Burst Read figures in the Micron data sheets show data output in portions, in response to (and synchronously with respect to) rising and falling edge transitions of the external clock signal." Murphy Decl. ¶ 87. Mr. Murphy then cites to various pages of Micron's data sheets without explaining the significance of those citations.

With respect to Micron's DDR2 products, Mr. Murphy cites to two pages of the data sheet. He pulls from a feature summary that the DRAM features a DLL "to align DQ and DQS transitions with CK." Murphy Decl. ¶ 87 (citing Micron DDR2 at 1). He then refers to a page of the data sheet showing burst read operations, which the court reproduces below. *Id.* (citing Micron DDR2 at 41).

[13] Mr. Murphy provides one paragraph of testimony noting that Micron's DDR2 SDRAM must "align with the external clock signal within t_{DQSS}." Murphy Reply Decl. ¶ 22. That paragraph quotes the datasheet, but fails to explain the significance of that parameter. More significantly, Mr. Murphy fails to make a similar showing as to the timing relationship in any other accused product. Thus, even if this showing sufficed as to Micron's DDR2 SDRAMs, the court could not enter summary judgment of infringement against any other device.

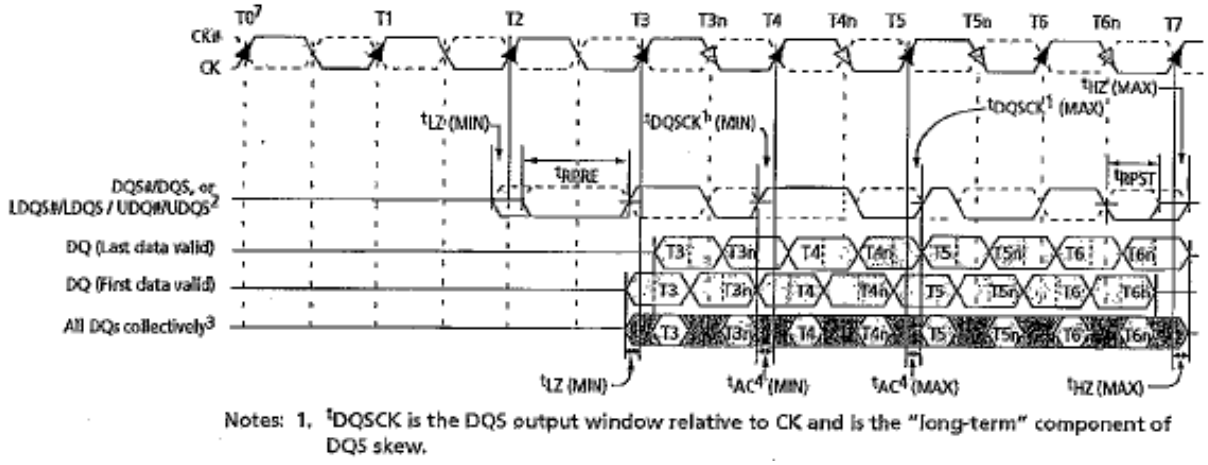


Notes: 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.

The read operation depicted above has a CAS latency of 4, hence the read operation begins four clock cycles after the read command is received by the DRAM. Thus, looking ahead to "T4," it appears that a differential clock transition, a DQS transition, and the transmission of data on the DQ lines all begin simultaneously. One could therefore read this datasheet as Mr. Murphy suggests as showing that data is output "in response to (and synchronously with respect to) rising and falling edge transitions of the external clock signal." Murphy Decl. ¶ 87. But one could equally infer that the data is output synchronously with respect to the transitions of the DQ strobes, or with the rising and falling transitions of both the external clock signal and the DQ strobes.

Easily overlooked in this figure is the qualification in note 5: "shown with nominal . . . t_{DQSCK}, t_{DQSQ}." The Micron DDR2 data sheet explains this caveat in a later figure, shown (in part) below:

Figure 29: Data Output Timing – tAC and tDQSCK



Notes: 1. tDQSCK is the DQS output window relative to CK and is the "long-term" component of DQS skew.

Micron DDR2 at 48. This figure demonstrates the indefinite nature of the figure Mr. Murphy relies upon in support of his conclusion. With various parameters set to "nominal," the timing of various actions inside the DRAM appear simultaneous. In reality, the relationship between the external clock signals, the data strobes, and the output of data is much more complex. It appears that the DDR2 SDRAM outputs data in response to the data strobe. It also appears that the data strobe adheres to the external clock signal within a parameter, t_{DSQCK}, but that the data strobe jitters about the external clock signal's transitions, sometimes preceding it (e.g., at T4) and sometimes lagging it (e.g., at T5).

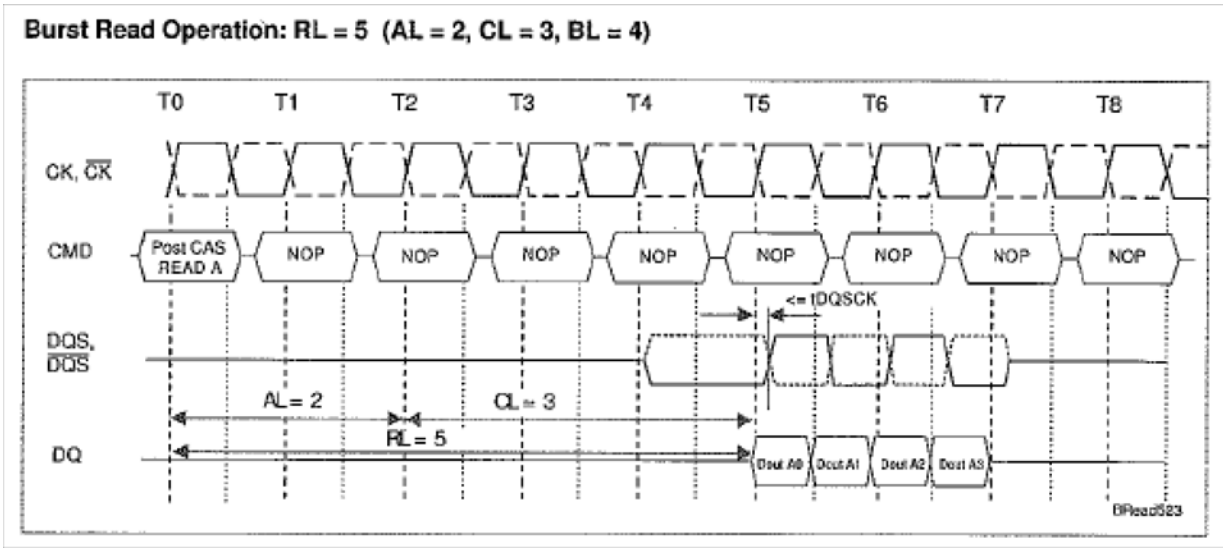
None of this complexity is made clear by Mr. Murphy's conclusory statement that the Micron DRAMs output data "(synchronously with respect to) rising and falling edge transitions of the external clock signal." The court accepted Rambus's cosntruction that for an event to occur "synchronously with respect to" a transition of an external clock signal, the event must be shown to have a "known timing relationship" with respect to the clock signal. Mr. Murphy's declaration – Rambus's basis for its summary judgment motion – makes no showing of what that "known timing relationship" is.

A further example of the weakness of Mr. Murphy's declaration lies in its "discussion" of Micron's DDR3 parts. Mr. Murphy supports his conclusion that they infringe by citing "Micron

DDR3 at Data Sheet at 2 ('The read data is transmitted by the DDR3 SDRAM edge-aligned to the data strobes')." This citation reflects that Micron's DDR3 transmits data with respect to the data strobes, and does not say anything with respect to the external clock signal. As discussed above, there appears to be a relationship between the data strobes and external clock signal, but Mr. Murphy does not explain what it is.

c. Nanya

Mr. Murphy's declaration is again too conclusory with respect to Nanya's products. It differs, however, from Mr. Murphy's description of Hynix and Micron's products in that Mr. Murphy states that "the figure[] entitled 'Burst Read Operation' in the Nanya DDR2 Data Sheet . . . show[s] data output in portions, in response to (and synchronously with respect to) rising and falling edge transitions of the external clock signal and the corresponding DQS and /DQS edges." Murphy Decl. ¶ 88. He again cites to a portion of a data sheet explaining that the data strobes are "edge aligned with read data." *Id.* (citing Nanya DDR2 at 4, 25). The cited diagram appears below:

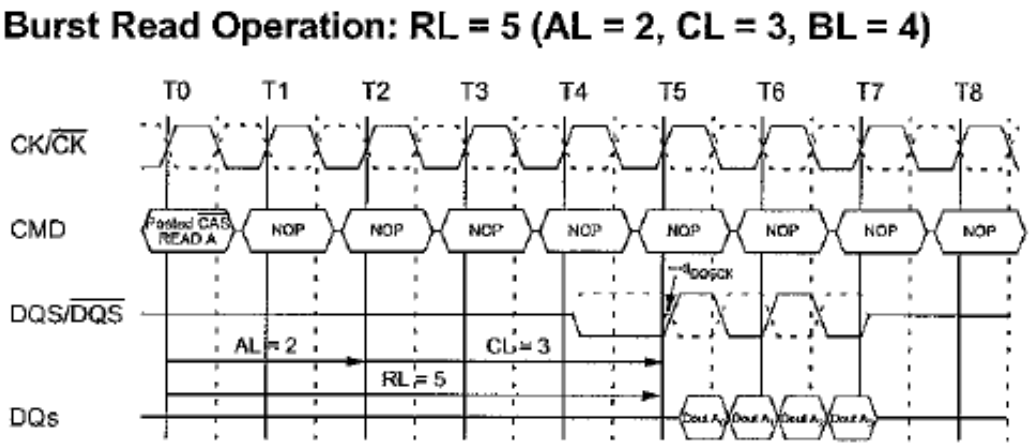


The diagram suggests that data output occurs simultaneously with the transitions of the differential clock signals. Again, however, it is unclear what the "known timing relationship" is between the external clock signal and the output of data.

d. Samsung

With respect to Samsung's products, Mr. Murphy reverts to the same conclusion he shared

with respect to Hynix and Micron: "The Burst Read figures in the Samsung documentation show data output in portions, in response to (and synchronously with respect to) rising and falling edge transitions of the external clock signal." Murphy Decl. ¶ 89. For Samsung's DDR2 parts, Mr. Murphy supports this conclusion with a single citation to a diagram. *See id.* (citing Samsung DDR2 Operation at 18).



Drawing all inferences in favor of Samsung, it is impossible (at least to the court's understanding) to discern the "known timing relationship" between data output and the external clock signal merely by glancing at this diagram. It appears that a transition of the differential clock signals triggers a transition of the DQ strobes, and shortly thereafter data is output.

3. Conclusion

In the end, the truth appears to be somewhere between the opinions of Mr. Murphy and Mr. McAlexander. The distinction between the external clock signal and DQ strobe is more than trivial. It appears that DQ strobe was added to the DDR generations of SDRAMs to decouple the timing of the data busses connecting a DRAM to a memory controller from the timing of the control and address busses. Jacob, *Memory Systems*, at 404-06. Because the control and addresses busses connect the memory controller to every DRAM in the environment (while a memory controller connects to each DRAM with a specific data bus), they must transmit more information farther, requiring lower clock frequencies. Using DQ strobes only on the data busses frees the data busses to operate at higher frequencies (and thus transmit more information). Obviously, activity on the data

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busses should still correspond to the activity on the command busses, hence the apparent need for a relationship between DQ strobe and the external clock signal. *See id.* at 407 ("Theoretically, the DQS signal, in its function as the source-synchronous clocking reference signal, operates independently from the global clock signal. However, where the DQS signal does operate independently from the global clock signal, the DRAM memory controller must either operate asynchronously or devote additional stages to buffer read data returning from the DRAM devices. A complete decoupling of the DQS signal from the global clock signal is thus undesirable.").

Whether this relationship is a "known timing" relationship cannot be determined on the present record, however, due to Rambus's insufficient showing. Mr. Murphy's declaration contains no discussion of the nature of the timing relationship between the clock signal, DQ strobe, and the output of data. His conclusion that the "synchronously with respect to" claim limitation is met is not enough. Accordingly, this issue will have to be decided based on the additional evidence presented at trial. Rambus's motion for summary judgment of infringement on these two claims is therefore denied.

4. Claim 36 of the '020 Patent

One of Rambus's asserted claims raises similar factual issues to those discussed above. Claim 36 of U.S. Patent No. 6,378,020 recites an integrated circuit device that outputs data "in response to" a rising and falling transition of an external clock signal. Mr. Murphy relies on the same discussion in paragraphs 86 to 89 of his declaration to support his conclusion that the Manufacturers' products meet this limitation. *See* Murphy Decl. ¶¶ 448, 452, 456, 460 (citing ¶¶ 86-89). As discussed, it appears that data is output in response to transitions in the DQ strobe signal. Mr. Murphy's declaration fails to establish the relationship between the external clock signal and the DQ strobe, and how the external clock signal might cause a transition in DQ strobe such that it could be said that the external clock signal's transition also caused the output of data. The court therefore denies Rambus's motion for summary judgment of infringement with respect to claim 36 as well.

B. Claim 14 of the '184 Patent, Claim 27 of the '051 Patent, and Claim 16 of the '863 Patent

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Three of Rambus's asserted claims contain a limitation similar to that discussed above, but this limitation relates to the input of data. For the reasons discussed below, Rambus has failed to carry its burden of production on infringement with respect to this limitation. The court therefore denies Rambus's motion for summary judgment with respect to claim 14 of U.S. Patent No. 6,182,184, claim 27 of U.S. Patent No. 6,314,051, and claim 16 of U.S. Patent No. 6,452,863.

1. The Asserted Claims Covering Data Input

Claim 14 of the '184 patent covers a method of operating a DRAM in which the DRAM receives a write request and samples "a first portion of the first amount of data synchronously with respect to a first transition of an external clock signal." U.S. Patent No. 6,182,184, col. 25, l. 57 – col. 26, l. 6. Claim 27 of the '051 patent claims a DRAM featuring "data input receiver circuitry to sample the first portion of data synchronously with respect to the external clock signal." U.S. Patent No. 6,314,051, col. 26, ll. 30-42. Finally, claim 16 of the '863 patent recites a method of operating a memory device in which the input of data to the DRAM "includes receiving the first amount of data synchronously with respect to the external clock signal." U.S. Patent No. 6,452,863, col. 25, ll. 43-64. The court adopted Rambus's proposed construction that "synchronously with respect to" means "having a known timing relationship with respect to." *Rambus*, 569 F. Supp. 2d at 986-87. Thus, to establish infringement of these three claims, Rambus must produce evidence that the accused DRAMs' sample incoming data with a "known timing relationship" to the transitions of the external clock signal.

2. Rambus's Proffer of Evidence Regarding Data Input Timing

For reasons identical to those discussed above, Rambus's proffer of Mr. Murphy's testimony is deficient. Mr. Murphy's opinion that the various Manufacturers infringe these data input claims are all based on his testimony in paragraphs 86-89 of his declaration. *See* Reply at 7; Murphy Decl. ¶¶ 113, 118, 123, 128, 181, 186, 191, 196; *but see* Murphy Decl. ¶¶ 510, 515.

Mr. Murphy's reliance on merely looking at the timing diagrams to support the existence of a "known timing relationship" is further belied in the case of write operations sending data to the DRAM, as opposed to reading it out of the DRAM. Unlike read operations (which are "edge

aligned" with DQ strobe), write operations are "center aligned" as shown in the following figure from a Hynix data sheet:

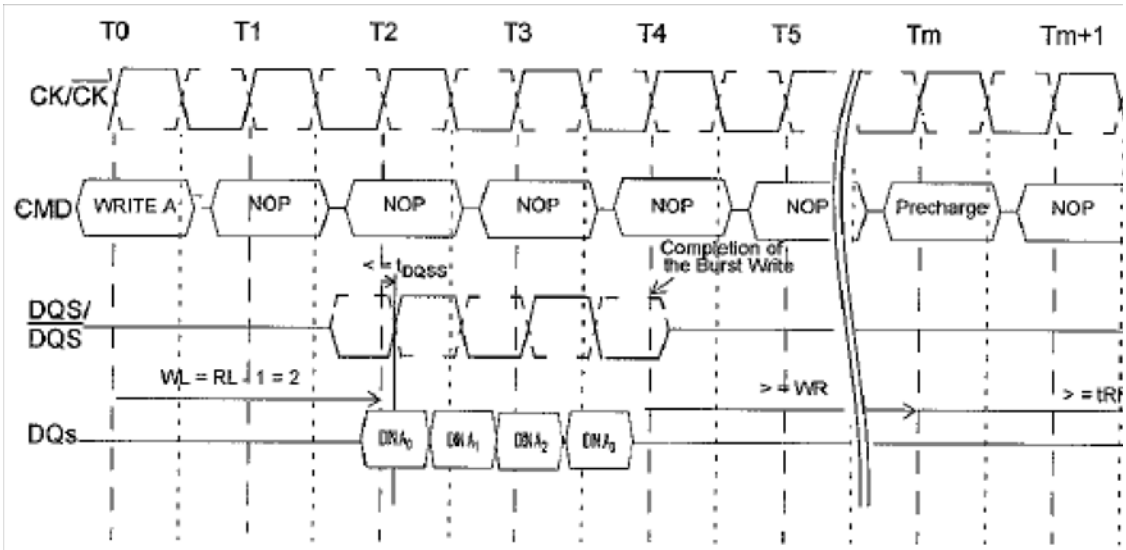

Figure 26. Burst write operation: RL = 3(AL=0, CL=3), WL = 2, BL = 4

Hynix DDR2 Operation at 27 (cited in Murphy Decl. ¶ 86). The only obvious inference that can be drawn from the diagram alone is that signals on the data pins (DQs) align their midpoint with the transitions of the DQ strobes. What "known timing relationship" the data input signals have to the clock signal is not clear.

3. Conclusion

As discussed above, Mr. Murphy's declaration is simply too conclusory to establish *facts* supporting an unequivocal, *prima facie* case that the Manufacturers' devices embody the various limitations requiring inputting data "synchronously with respect to" ("having a known timing relationship with respect to") the external clock signal. It may be that Rambus will be able to make this showing at trial, but it has not done so sufficiently on summary judgment. Accordingly, the court denies Rambus's motion for summary judgment on these three claims.

C. Claims With "Synchronous" Limitations

1. The Asserted Claims

The preamble of the majority of Rambus's asserted claims indicate that claims are directed to a "synchronous integrated circuit device," "synchronous memory device," or "synchronous dynamic

random access memory." U.S. Patent Nos. 6,314,051 (claim 43); 6,324,120 (claim 33); 6,426,916 (claim 28); 6,452,863 (claim 16); 6,546,446 (claim 3); 6,584,037 (claim 34); and 6,751,696 (claim 4). The court adopted Rambus's construction of the "synchronous" adjective as requiring that the device "receive[] an external clock signal which governs the timing of the response to a transaction request." *Rambus*, 569 F. Supp. 2d at 987. A "transaction request" is "a series of bits used to request performance of a transaction with a memory device." *Id.* at 984-85. To establish infringement of these claims, Rambus must put facts into evidence showing that the Manufacturers' accused devices receive an external clock signal that governs the timing of their response to a transaction request.

2. Rambus's Proffer

Mr. Murphy describes why he believes that the Manufacturers' products are "synchronous" devices early in his declaration. *See* Murphy Decl. ¶¶ 45-48. Mr. Murphy correctly points out that all of the Manufacturers' data sheets refer to their corresponding products as "synchronous" DRAMs. *See id.* Mr. Murphy loses sight, however, of the claim construction that Rambus proposed (and he endorsed). As used in the claims, a "synchronous" memory device must receive an external clock signal *governing* the timing of its response to a transaction request. Mr. Murphy's declaration does not lay out facts establishing that the accused devices' responses to transaction requests are "governed" by the external clock signal. *See id.* Indeed, as discussed above, it appears that the DRAMs input and output data in response to the devices' DQ strobe signals, not an external clock signal, and Rambus has failed to produce sufficient evidence of the relationship between the DQ strobes and the clock signal to warrant summary judgment. Rambus has similarly failed to present facts establishing that the external clock signal "governs" the DRAMs' responses to transaction requests. Accordingly, Rambus's motion for summary judgment of infringement with respect to these claims is denied.

IV. REJECTED ARGUMENTS

The Manufacturers' opposition raises eleven non-infringement arguments, of which the court has discussed nine. The final two arguments amount to issues of claim construction given that there

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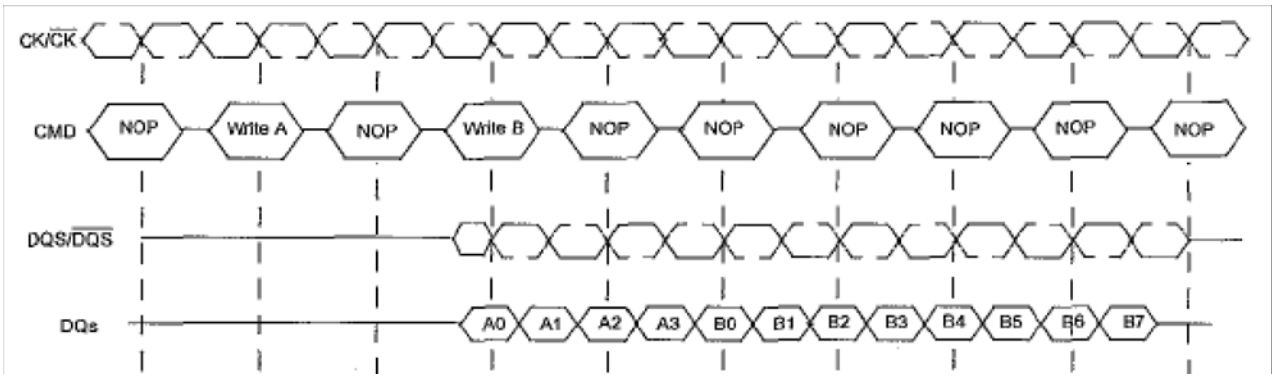
is no debate as to how the Manufacturers' DRAMs function.

A. "Block Size Information"

A variety of Rambus's claims, for example, claim 14 of U.S. Patent No. 6,182,184, include a limitation requiring the device to receive a "first block size information from a master, wherein the first block size information defines a first amount of data to be sampled by the memory device in response to a write request." The court has construed "block size information" to mean "[i]nformation that specifies the total amount of data that is to be transferred on the bus in response to a transaction request." *Rambus*, 569 F. Supp. 2d at 976 & App'x 2. This secondary claim construction dispute turns on the meaning of "specifies the total amount of data."

There is no dispute about how the accused DRAMs function. The court uses Hynix's DDR2 SDRAM to illustrate. Hynix's DDR2 SDRAM can operate with burst lengths of 4 or 8. Hynix DDR2 at 4; Hynix DDR2 Operation at 6. The burst length determines the duration of the write operation, i.e., a burst length of 8 corresponds to a burst lasting eight half clock cycles and permitting eight bits of data to be transferred. *See* Hynix DDR2 Operation at 4, 24. This implies that the DRAM will send or receive 8 bits of information on each data line. Murphy Decl. ¶ 66; McAlexander Decl. ¶ 73. Like the CAS and additive latency values, the burst length parameter resides in the programmable mode register, where it is programmed when the device is turned on. Hynix DDR2 Operation at 5-6.

But things can happen that prevent the DRAM from receiving the maximum amount of data in response to a write request. For example, the memory controller can interrupt a write command, truncating the amount of data received by the DRAM. McAlexander Decl. ¶ 75. This is shown in the figure below:



Hynix DDR2 Operation at 30. In the figure, the initial write command is represented by the hexagon labeled "Write A." The DRAM in this example has been programmed with a write latency of 2, meaning the that the write operation begins two clock cycles after the DRAM receives the write command, thus the DRAM begins receiving the bits corresponding to the Write A command (labeled A0, A1 . . .A3) two clock cycles later. Exactly two clock cycles following the Write A command, the Hynix DDR2 may also receive a second write command from the memory controller, "Write B." *Id.*[14] Two clock cycles following the receipt of Write B, the DRAM begins receiving the data labeled B0, B1 . . . B7, truncating the Write A transaction. Thus, despite having been programmed with a burst length of 8, the DRAM only received 4 bits of data per pin in response to the Write A command.

The Manufacturers first argue that because the memory controller can interrupt a write command, the burst length cannot "specify" the total amount of data to be transferred. That the memory controller possesses the ability to interrupt only a subset of write operations reveals that this non-infringement argument has no merit. There is no dispute that when the DDR2 devices are programmed by the memory controller with a burst length of four, the write operation cannot be interrupted and will always be 4 bits long. Moreover, when the DDR2 device is programmed with a burst length of eight and *not* interrupted, there is no dispute that the write operation will always be 8

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[14] In the Hynix DDR2, an interrupting write command may only be sent two clock cycles after an initial write command. Write interrupts are not permitted at any other time. Hynix DDR2 Operation at 29. Also, write operation interrupts are only possible when the DRAM uses an 8-bit burst length. *Id.*

bits long. Although there are instances in the operation of a DDR2 SDRAM when the memory controller interrupts the write operation and the device arguably no longer practices the claimed method of operating a memory device, the fact that a device possesses a non-infringing mode of operation does not mean that the device never performs an infringing method. *Hilgraeve*, 265 F.3d at 1343 ("[T]he sale of a device may induce infringement of a method claim, even if the accused device is capable of non-infringing modes of operation in unusual circumstances"). On the contrary, the undisputed evidence is that outside of the narrow circumstances of an interrupted write command, the memory device receives burst length information that indicates the amount of data to be sampled in response to a write request.

The Manufacturers also argue that the burst length parameter does not specify the "total" amount of data to be transferred on the bus in response to a write request. The burst length value received by the DRAM dictates the amount of data to be transferred on a single data line, not the entire data bus. McAlexander Decl. ¶¶ 73-74, 80. Mr. McAlexander therefore opines that the burst length value cannot specify the "total" amount of data. *Id.* ¶ 80. Mr. Murphy agrees that the burst length value does not *equal* the total amount of data, but opines that it does "specify" the total amount of data because the total amount of data to be transferred in response to a write command (outside of contexts where the write command is interrupted) is equal to the burst length multiplied by the number of data pins.

This is not a factual dispute about the operation of the accused devices, but rather an argument about the proper interpretation of the court's claim construction. The question is whether information that "specifies" a value must *equal* that value, or simply be able to produce that value by a function. The court previously considered this argument in the prior *Hynix* case and held that the burst length "specifies" the total amount of information to be transferred because it "represents (specifies) the total amount of data to be transferred." Block Size Order at 3-4. The court confirms this holding. Although the burst length value transmitted by the memory controller to a DRAM when the DRAM is initialized does not *equal* the total amount of information to be transferred in response to transaction requests, it does *specify* the total amount of information to be transferred

because the total amount of information is a scalar function of the burst length value.

Accordingly, the court concludes that Rambus has met its burden of producing evidence showing that the devices accused of infringing claims with block size limitations embody those limitations.[15]

B. Sampling an Operation Code In Response To a Rising/Falling Edge

One asserted claim (claim 4 of the '696 patent) recites a synchronous memory device that includes "input receiver circuitry to sample a first operation code in response to a rising edge transition of the external clock signal." Rambus met its burden of production with respect to a similar limitation by showing how the accused DRAMs receive a request for a write operation in a known timing relationship to the external clock signal. *See supra*, III-A-2-c (citing, among other things, Murphy Decl. ¶ 76).

Here, the Manufacturers argue that the DRAMs do nothing in response to the rising edge transition of the external clock signal, but rather respond only to the crossing points of a differential clock signal. But the differential clock signal is composed of two clock signals, CK and CK\, and its crossing points are the result of the falling and rising edges of CK and CK\. Thus, the accused DRAMs do sample an operation code "in response to a rising edge transition of the external clock signal." That rising edge transition, in combination with the falling edge transition of CK\, create the crossing point of the differential clock that causes the DRAM to sample the operation code.

V. ORDER

For the foregoing reasons, the court rules as follows:

1. The court grants partial summary judgment with respect to claim 16 of the '285 patent. Rambus has established that any use of the devices accused of infringing this claim (except for Nanya's DDR3 SDRAM) directly infringes claim 16.

2. The court denies summary judgment as to claim 4 of the '696 Patent and claim 3 of

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[15] In passing, the Manufacturers argue that there is a triable issue of fact because Mr. McAlexander disagrees with Mr. Murphy that the burst length value reads on the "block size" limitation of the claim. As discussed in section II, this "unsupported conclusion" alone does not carry the Manufacturer's burden of setting forth evidence of a factual dispute.

the '446 Patent.

3. The court denies summary judgment as to claim 36 of the '8,020 Patent.

4. The court denies summary judgment as to claim 14 of the '184 Patent, claim 27 of the '051 Patent, and claim 16 of the '863 Patent.

5. The court denies summary judgment as to the remaining "synchronous" claims: claim 43 of the '051 Patent; claim 33 of '120 Patent; claim 28 of '916 Patent; and claim 34 of '037 Patent.

6. The court grants partial summary judgment over the Manufacturers' arguments related to claim construction disputes as described in the order. The disputes resolved are the arguments numbered 1, 2, 3, 4, and 8 in the Manufacturers' opposition brief.

DATED: 11/24/2008

Ronald M. Whyte

RONALD M. WHYTE
United States District Judge

United States District Court
For the Northern District of California

Notice of this document has been electronically sent to counsel in:

C-05-00334, C-05-02298, C-06-00244.

Counsel	Email	Appearances:		
		05-00334	05-02298	06-00244
Elpida:				
Eric R. Lamison	elamison@kirkland.com	x		
Hynix:				
Theodore G. Brown , III	tgbrown@townsend.com	x	x	x
Karin Morgan Cogbill	kfrenza@thelen.com, pawilson@thelen.com	x		x
Daniel J. Furniss	djfurniss@townsend.com	x		
Joseph A. Greco	jagreco@townsend.com	x		
Julie Jinsook Han	JJHan@townsend.com	x	x	x
Tomomi Katherine Harkey	tharkey@omm.com	x		
Jordan Trent Jones	jtjones@townsend.com	x		
Patrick Lynch	plynch@omm.com	x		
Kenneth Lee Nissly	kennissly@omm.com	x		x
Kenneth Ryan O'Rourke	korourke@omm.com	x		
Belinda Martinez Vega	bvega@omm.com	x	x	x
Geoffrey Hurndall Yost	gyost@thelenreid.com	x	x	x
Susan Gregory van Keulen	svankeulen@omm.com	x		x
Interdigital:				
Nathan Loy Walker	nathan.walker@wilmerhale	x		
Micron:				
Robert Jason Becher	robertbecher@quinnemanuel.com	x		x
John D Beynon	john.beynon@weil.com	x	x	x
Jared Bobrow	jared.bobrow@weil.com	x	x	x
Yonaton M Rosenzweig	yonirosenzweig@quinnemanuel.com	x		x
Harold Avrum Barza	halbarza@quinnemanuel.com			x
Linda Jane Brewer	lindabrewer@quinnemanuel.com			x
Aaron Bennett Craig	aaroncraig@quinnemanuel.com			x
Leeron Kalay	kalay@fr.com			x
David J. Lender	david.lender@weil.com			x
Rachael Lynn Ballard McCracken	rachaelmccracken@quinnemanuel.com			x
Sven Raz	sven.raz@weil.com			x
David J. Ruderman	davidruderman@quinnemanuel.com			x
Elizabeth Stotland Weiswasser	elizabeth.weiswasser@weil.com			x
Nanya:				
Jason Sheffield Angell	jangell@orrick.com	x	x	x
Kristin Sarah Cornuelle	kcornuelle@orrick.com	x	x	x
Chester Wren-Ming Day	cday@orrick.com	x		
Jan Ellen Ellard	jellard@orrick.com	x		x
Vickie L. Feeman	vfeeman@orrick.com	x	x	x
Robert E. Freitas	rfreitas@orrick.com	x		
Craig R. Kaufman	hlee@orrick.com	x		
Hao Li	hli@orrick.com	x		

Cathy Yunshan Lui	clui@orrick.com	x		
Theresa E. Norton	tnorton@orrick.com	x		
Mark Shean	mshean@orrick.com	x		
Kaiwen Tseng	ktseng@orrick.com	x		
Rambus:				
Kathryn Kalb Anderson	Kate.Anderson@mto.com	x		x
Peter A. Detre	detrepa@mto.com	x	x	x
Erin C. Dougherty	erin.dougherty@mto.com	x	x	x
Sean Eskovitz	sean.eskovitz@mto.com	x	x	x
Burton Alexander Gross	Burton.Gross@mto.com	x	x	x
Keith Rhoderic Dhu Hamilton, II	keith.hamilton@mto.com	x	x	x
Pierre J. Hubert	phubert@mckoolsmith.com	x	x	x
Andrea Jill Weiss Jeffries	Andrea.Jeffries@mto.com	x	x	x
Miriam Kim	Miriam.Kim@mto.com	x	x	x
Carolyn Hoecker Luedtke	carolyn.luedtke@mto.com	x	x	x
Steven McCall Perry	steven.perry@mto.com	x	x	x
Jennifer Lynn Polse	jen.polse@mto.com	x	x	x
Matthew Thomas Powers	mpowers@sidley.com	x		
Rollin Andrew Ransom	rransom@sidley.com	x	x	x
Rosemarie Theresa Ring	rose.ring@mto.com	x	x	x
Gregory P. Stone	gregory.stone@mto.com	x	x	x
Craig N. Tolliver	ctolliver@mckoolsmith.com	x	x	x
Donald Ward	Bill.Ward@mto.com	x	x	x
David C. Yang	david.yang@mto.com	x	x	x
Douglas A. Cawley	dcawley@mckoolsmith.com			x
Scott L Cole	scole@mckoolsmith.com			x
Samsung:				
Steven S. Cherensky	steven.cherensky@weil.com	x	x	
Claire Elise Goldstein	claire.goldstein@weil.com	x	x	
Dana Prescott Kenned Powers	dana.powers@weil.com	x	x	x
Matthew Douglas Powers	matthew.powers@weil.com, matthew.antonelli@weil.com	x	x	
Edward Robert Reines	Edward.Reines@weil.com	x	x	
Texas Instruments:				
Kelli A. Crouch	kcrouch@jonesday.com	x	x	x

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Dated: 11/24/2008

TSF
Chambers of Judge Whyte